LED Driver Achieves Electrolytic Capacitor-Less and Flicker-Free Operation with an Energy Buffer Unit

Peng Fang, Member, IEEE, Bo Sheng, Member, IEEE, Sam Webb, Student Member, IEEE, Yan Zhang, Member, IEEE, Yan-Fei Liu, Fellow, IEEE

Abstract—Electrolytic capacitors are often needed to provide the high-density energy storage required by AC powered LED drivers, however, they are also well known for their short lifespans. Eliminating electrolytic capacitors in AC-DC LED driver design has become a very important target to improve LED driver technology. In this paper, a cycle-by-cycle energy buffering LED driver has been proposed to achieve electrolytic capacitor-less flicker-free operation. An energy buffering unit (EBU), with high voltage film capacitors being the energy storage device, is introduced in the design to buffer the imbalanced energy in every switching cycle. The switching current can be controlled to meet high power factor correction requirement while maintaining DC LED output current at the same time. Compared to previous electrolytic capacitor-less designs, this technology can reduce circulating power and, therefore, power conversion loss. A 15W experimental prototype had been built and tested to verify the proposed LED driving method.

Index Terms—Cycle by cycle energy buffering, Electrolytic Capacitor-less design, LED Driver, Flicker-free operation

I. INTRODUCTION

LED lighting has been steadily increasing in popularity, owing largely to its high efficacy, long lifespan, and environmentally-friendly operation. It is replacing fluorescent lighting and becoming the primary artificial lighting sources in many applications. Although having inherent advantages over fluorescent lighting, there are several technical challenges that need to be overcome to fully take advantage of LED lighting, particularly with the AC powered LED driver. In an AC connected driver, the notorious double-line-frequency flicker, which can cause numerous health issues, will occurs unless the driver is properly designed to eliminate it. Therefore, the key to realizing the full benefits of LED lighting lies in LED driver designs. Also, LED drivers heavily determine the size, efficiency, and cost of LED lighting fixtures, playing a critical role in LED lighting deployment.

EnergyStar requires power factor correction (PFC) to be implemented for lighting devices higher than 5W. The power factor must be higher than 0.9 for commercial usages and 0.7 for residential usages [1], which results in a time-varying input power with a double-line-frequency ripple, as shown in Fig. 1. On the other side, achieving flicker-free LED driving requires constant output power. Therefore, energy buffering for double-line-frequency imbalanced energy is required. Conventional single-stage LED driver uses the simplest form of energy buffering, by paralleling bulky electrolytic capacitors at its output. Part of the ripple power is buffered by the storage capacitor while the remaining escapes to the LED load and, therefore, generates double-line-frequency flicker. Only an infinitely large storage capacitor can buffer 100% of the ripple power using this technique. Thus, double-line frequency flicker is always present with single-stage LED driver based design. The recommended low-risk flicker level should be less than 0.08\% flicker percent of the average [3], which is equivalent to 10\% for 120Hz flicker (under 60Hz mains) and 8\% for 100Hz flicker (under 50Hz mains), respectively. Commercially available single-stage LED drivers usually exceed the recommended safe level.

Fig. 1 Energy imbalance between AC input power and expected LED output power with grid-connected LED drivers

Double-line-frequency flicker raises health-related concerns. Although usually not visible, it can be picked up by retina that leads to visual fatigue and other problems [4], [5]. Conventional two-stage LED drivers can naturally achieve flicker-free LED driving. The additional DC-DC stage in a two-stage design can filter the double-line-frequency ripple power. The drawback is additional loss from the extra power stage and higher cost due to the additional components.

A variety of LED driving methods have been investigated to achieve flicker-free LED driving performance while maintaining high efficiency, and low cost. Some focus on novel control strategies while others focus on power topologies. For
instance, the harmonic current injection method had been proposed to reduce imbalanced energy in a half line cycle [6]. Similar methods include input or output current shaping [7]-[9]. They can lessen the severity of flicker but cannot completely remove it. There are also two-stage integration methods [10]-[12] that share components between the first and the second power stages, leading to a reduction in component count and lower cost. However, optimal operation is difficult to achieve because of extra constraints from component sharing. Ripple cancellation methods [14]-[18] have also been proposed to achieve flicker-free operation. An opposite ripple voltage is produced to cancel the double-line-frequency ripple voltage from main PFC circuit. A DC LED voltage and LED current can be produced to achieve flicker-free operation. This method can achieve very good efficiency and reduce requirement on storage capacitors. It is possible to achieve electrolytic capacitor-less design, but only for high LED output voltage applications [17].

High voltage film capacitors have sometimes been used as storage capacitors to replace electrolytic capacitors. Electrolytic capacitors are often used as high-density energy storage device, buffering the double-line-frequency imbalanced energy. However, it compromises system life. Like other semiconductor devices, LEDs can last for decades. On the other side, the lifespan of electrolytic capacitors is an order of magnitude less [19]. Therefore, eliminating them in LED driver designs becomes paramount. The lifespan of electrolytic capacitors is an order of magnitude less [19]. Therefore, eliminating them in LED driver designs becomes paramount.

Eliminating the need for a secondary side control circuit can increase efficiency and reduces cost. Primary side control can be easily implemented with the proposed LED driver. The signals required to build the LED current regulation loop can be sensed at the primary side. Control scheme is discussed in section V. The design procedure and consideration are discussed in section VI. The simulation and experimental result are presented in section VII and finally, the paper is concluded in section IX.

The remaining part of this paper is organized as follows. Section II presents the design concept and operating principle of the proposed LED driver. Section III discusses the component requirement. Control scheme is discussed in section IV and the loss analysis is provided in Section V. The design procedure and consideration are discussed in Section VI. The simulation and experimental result are presented in Section VII and finally, the paper is concluded in Section IX.
II. DESIGN CONCEPT AND OPERATING PRINCIPLE

For a conventional single-stage LED driver, power factor correction and DC LED output power cannot be achieved at the same time. A Flyback LED driver operating under discontinuous current conduction mode (DCM) is used as an example to illustrate this point. Fig. 4(a) shows the primary side and the secondary side switching current, $I_{pri}$ and $I_{sec}$, of a conventional Flyback LED driver when power factor correction is performed. Fig. 4(b) shows the required primary side and secondary side switching current that can deliver constant LED output current. As shown, performing power factor correction requires the peak primary side switching current to follow the input voltage. On the contrary, delivering constant LED output power requires identical secondary side switching current in every switching cycle. Therefore, the switching current waveforms need to be changed to bridge the different requirements of these two.

![Fig. 4 Primary side and secondary side switching current waveforms, (a) conventional Flyback LED driver with PFC implementation, (b) expected waveforms to achieve constant LED current output](image)

Fig. 5 shows two different patterns of switching current when $P_{in} > P_{LED}$. Fig. 5(a) represents the waveforms in a conventional design. When power factor correction is performed, the peak primary side switching current is higher than $I_{pri\_req}$, which is the amount required from LED output. Fig. 5(b) shows the conceptual change on the switching current. The current drawn from AC input happens in two occasions and the area A1 (or A2) and B1 (or B2) are used to represent them. When the primary side switching current hits $I_{pri\_req}$, the primary side current is ended as the switch controlling it is turned off. The magnetic current commutes to the secondary side and the extra amount of current is delivered to the LED output. When $I_{sec}$ becomes zero, more primary side current is drawn from AC input, as represented by area A1, for power factor correction. In this condition, the peak primary side switching current is still lower than $I_{pri\_req}$. As the current drawn from AC input is the same in both cases, the power factor correction performance is maintained. The primary side switching current stops when it hits $I_{pri\_req}$. The extra current supplied by the conceptual source also means extra energy supplied by the conceptual source.

![Fig. 5 Illustration of switching current when $P_{in} > P_{LED}$, (a) conventional design waveforms, (b) conceptual waveforms achieve energy buffering](image)

A storage capacitor can serve as the voltage source when $P_{in} < P_{LED}$. It can also serve as the load when $P_{in} > P_{LED}$. Therefore, in every switching cycle, the imbalanced energy is buffered by the energy storage capacitor. To achieve the above current repatterning concept, an interfacing circuit needs to be designed between the storage capacitor and a conventional LED driver and the proposed LED driver is shown in Fig. 7.

![Fig. 6 Illustration of switching current when $P_{in} < P_{LED}$, (a) conventional design waveforms, (b) conceptual waveforms achieve energy buffering](image)
The power stage is based on the Flyback topology with an extra energy buffer unit (EBU) to achieve high power factor and constant current output in every switching cycle. When \( P_{in} < P_{LED} \), the additional energy is supplied from the storage capacitor, \( C_{sto} \), to the LED load. When \( P_{in} > P_{LED} \), the extra energy is stored into \( C_{sto} \). The output capacitor \( C_{oi} \) is implemented by a 10\( \mu \)F ceramic capacitor in the experimental prototype to filter the switching frequency ripple. The storage capacitor, \( C_{sto} \), is implemented with a 2 \times 3.3\( \mu \)F, 450V film capacitor. The switching operations during \( P_{in} < P_{LED} \) and \( P_{in} > P_{LED} \) are different and they will be discussed separately.

**A. Operation when \( P_{in} < P_{LED} \)**

The LED driver is operated under discontinues conduction mode (DCM) with four distinct time intervals, \([t_0-t_1] , [t_1-t_2] , [t_2-t_3] , [t_3-t_4] \) in one switching cycle. The critical switching waveforms are shown in Fig. 8.

During \([t_0-t_1] \)

Fig. 9(a) illustrates the circuit operation during the time interval \([t_0-t_1] \) when \( P_{in} < P_{LED} \). The MOSFET \( Q_1 \) is turned on at \( t_0 \) and current is drawn from the AC input. Because the primary side winding, \( N_{pri} \), is oriented in Flyback mode with respect to the secondary side windings, \( N_{sec} \), and buffer winding, \( N_{buf} \), the diode \( D_1 \), \( D_2 \) are reverse biased. During this time interval, \( Q_2 \) and \( Q_3 \) are off. The body diode of \( Q_2 \) is forward biased. The voltage on \( D_1 \) can be expressed as:

\[
V_{D1, (P_{in} < P_{LED})} \left[ t_0 - t_1 \right] = V_o + V_{in} \times \frac{N_{buf}}{N_{pri}}
\]

The voltage on diode \( D_2 \) can be expressed as:

\[
V_{D2, (P_{in} < P_{LED})} \left[ t_0 - t_1 \right] = V_o + V_{in} \times \frac{N_{buf}}{N_{pri}}
\]

The voltage, \( V_{sto} \), is designed to be higher than \( V_{in\_rec} \) when \( P_{in} < P_{LED} \). Therefore, the diode \( D_3 \) is forward biased, and the body diode of \( Q_3 \) is reverse biased. The voltage across \( Q_3 \) can be expressed as:

\[
V_{\theta, (P_{in} < P_{LED})} \left[ t_0 - t_1 \right] = V_o - V_{in\_rec}
\]

This interval ends at time \( t_1 \) when the switching current drawn from the AC input reaches the level required for power factor correction.

During \([t_1-t_2] \)

Fig. 9(b) illustrates the circuit operation during the time interval \([t_1-t_2] \). The MOSFET \( Q_3 \) is turned on at \( t_1 \) and \( Q_1 \) is remaining on. Because \( V_{sto} \) is higher than \( V_{in\_rec} \), the input
bridge rectifier is reversed biased, and there is no more current drawn from the AC input during this time interval. $C_{ac}$ provides the switching current in primary side winding instead. No AC input current during $[t_1-t_2]$ is desirable as enough AC current had been drawn for power factor correction during $[t_0-t_1]$. $D_1$ and $D_2$ are still reverse biased, and $Q_2$ is forward biased. As the voltage on the primary side winding becomes $V_{sto}$, the voltages on diode $D_1$ and $D_2$ during this time interval also change and become:

$$V_{D1(t_0<t_{LED})}[t_1-t_2] = V_o + V_t \frac{N_{pri}}{N_{sec}}$$

(4)

$$V_{D2(t_0<t_{LED})}[t_1-t_2] = V_s + V_t \frac{N_{buf}}{N_{pri}}$$

(5)

This time interval ends at time $t_2$ when the primary side switching current hits $I_{pri req}$, which represents the current level required for delivering a constant LED output current. $I_{pri req}$ is automatically generated by a feedback loop that will be discussed in Section V. Both $Q_1$ and $Q_3$ are turned off at $t_2$.

**During $[t_2-t_3]$**

Fig. 9(c) illustrates the circuit operation during the time interval $[t_2-t_3]$. As $Q_1$, $Q_3$ are turned off at $t_2$ and $Q_2$ is still off, the magnetic current is forced to commute from the winding $N_{pri}$ to the winding $N_{sec}$. The voltage on the secondary side winding is clamped at $V_o$ with ignoring the forward voltage drop on $D_1$. The voltage on the secondary side winding is reflected to the primary side winding and the buffer winding. The voltage across the primary side winding can be expressed as:

$$V_{N_{pri}(t_0<t_{LED})}[t_2-t_3] = V_o + \frac{N_{pri}}{N_{sec}}$$

(6)

The voltage on $Q_1$ can, therefore, be expressed as:

$$V_{Q1(t_0<t_{LED})}[t_2-t_3] = V_{in rec} + V_o + \frac{N_{pri}}{N_{sec}}$$

(7)

The voltage across winding $N_{buf}$ can be expressed as:

$$V_{N_{buf}(t_0<t_{LED})}[t_2-t_3] = V_o + \frac{N_{buf}}{N_{sec}}$$

(8)

In the proposed LED driver, $V_{sto}$ is designed to be always smaller than the voltage on the buffer winding during $[t_2-t_3]$ given by Eq. (8). Therefore, the diode $D_2$ is forward biased while the body diode of $Q_3$ is reverse biased. The voltage on $Q_3$ can be expressed as:

$$V_{Q3(t_0<t_{LED})}[t_2-t_3] = \max \{(V_{n rec} - V_{sto})\}$$

(9)

The status of $D_3$ and $Q_3$ is the same as it is in the interval $[t_0-t_1]$. The magnetic current in winding $N_{pri}$ starts decreasing at $t_2$ and becomes zero at $t_3$, which ends this time interval.

**During $[t_3-t_4]$**

An idle interval $[t_3-t_4]$ is followed to achieve DCM operation. No active switching operation happens in this interval.

**B. Operation when $P_o > P_{LED}$**

When $P_o > P_{LED}$, the extra energy is transferred from the AC input to the storage capacitor $C_{sto}$ in every switching cycle. Fig. 10 shows the key switching waveforms with one switching cycle being divided into five time intervals, $[t'0-t'1]$, $[t'1-t'2]$, $[t'2-t'3]$, $[t'3-t'4]$ and $[t'4-t'5]$.

![Key switching waveforms](image)

During $[t'0-t'1]$.

Fig. 11(a) shows the circuit operation during the time interval $[t_0-t_1]$ when $P_o > P_{LED}$. It is the same as Fig. 9(a) when $P_o < P_{LED}$. Therefore, (1) and (2) can be reused to describe voltage stresses of $D_1$ and $D_2$. The voltages on $Q_1$ and $Q_3$ are dependent on the instantons value of $V_{in rec}$ and $V_{sto}$. Both $V_{in rec}$ and $V_{sto}$ change in a half line cycle and the situation can change between $V_{in rec} > V_{sto}$ and $V_{in rec} < V_{sto}$. The voltage on $Q_3$ and $D_3$ can be expressed as:

$$V_{Q3(t_0>t_{LED})}[t_0-t_1] = \max \{(V_{n rec} - V_{sto})\}$$

(10)

and

$$V_{D3(t_0>t_{LED})}[t_0-t_1] = \max \{(V_{sto} - V_{max})\}$$

(11)

As $Q_3$ is always off when $P_o < P_{LED}$, the voltage stresses of $Q_3$ and $D_3$ remain unchanged in the entire switching cycle. At $t_3$, the primary side winding reaches $I_{pri req}$ and $Q_1$ is turned off. One should note that the current drawn from the AC input is not sufficient to perform power factor correction yet at $t_1$. More current will be drawn from AC input during the time interval $[t'2-t'3]$.

During $[t'1-t'2]$.

Fig. 11(b) shows the circuit operation during the time interval $[t_1-t_2]$ when $P_o > P_{LED}$. It is the same as Fig. 9(b). Therefore, (7) and (9) can be reused to describe voltage stress...
for each component. This interval ends at $t_2$ when the secondary side current drops to zero.

**During $[t_2-t_3]$**

Fig. 11(c) shows the circuit operation during the time interval $[t_2-t_3]$ when $P_{in} > P_{LED}$. $Q_1$ is turned on again at $t_2$ to draw more current from AC input. The voltage stresses of the components in $[t_2-t_3]$ are the same as they are in $[t_1-t_2]$. This time interval ends at $t_3$ when the exact amount of current required for power factor correction is drawn from AC input.

**During $[t_3-t_4]$**

Fig. 11(d) shows the circuit operation during the time interval $[t_3-t_4]$ when $P_{in} > P_{LED}$. Since $Q_1$ is turned off at $t_4$ and the $Q_2$ is already on, the magnetic current commutes from winding $N_{pri}$ to winding $N_{buf}$. The magnetic current does not flow in secondary side winding because of the following relationship in the design:

$$V_{sto} \times \frac{N_{sec}}{N_{buf}} < V_o$$  \hspace{1cm} (12)

When the magnetic current flows in winding $N_{buf}$, the voltage on the winding is clamped at $V_{sto}$. The term on the left side of the “less than” sign of (12) is equal to the voltage reflected to the secondary side winding at the time. Therefore, the LED output voltage during $[t_3-t_4]$ is higher than the secondary side winding voltage and the diode $D_1$ is reverse biased to block current. The voltage across $D_1$ can be expressed as:

$$V_{D1(\{P_{in} > P_{LED}\})} = V_o - V_{sto} \times \frac{N_{sec}}{N_{buf}}$$  \hspace{1cm} (13)

The voltage on the buffer winding is also reflected to the primary side winding, and the voltage on $Q_1$ can be expressed as:

$$V_{Q1(\{P_{in} > P_{LED}\})} = V_{in} + V_{sto} \times \frac{N_{pri}}{N_{buf}}$$  \hspace{1cm} (14)

This time interval ends at $t_4$ when the magnetic current in winding $N_{buf}$ decreases to zero.

**During $[t_4-t_5]$**

A small idle time interval $[t_4-t_5]$ is used to achieve DCM operation. No active switching operation happens in this interval.

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**C. Overall operation in a half line cycle**

Since the switching operations under both $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ have been discussed, the overall view of the operation in a half line cycle is illustrated in Fig. 12.

![Fig. 12 Switching operation over a half line cycle](image)

The above discussion also reveals that the imbalanced energy had only gone through two power conversion steps. When $P_{in} > P_{LED}$, the imbalanced energy is transferred from AC input side to the storage capacitor, directly. When $P_{in} < P_{LED}$, it
is then transferred from the energy storage capacitor to the LED output side. One less power conversion step is required with the proposed LED driver as compared to active filter and previous three-port LED drivers.

### III. COMPONENT REQUIREMENT ANALYSIS

#### A. Component Voltage Stress

As the expressions of the component voltage stresses have been derived in each time interval, the maximum voltage stress expression for them in a half line cycle are summarized and shown in TABLE 1. The maximum voltage stresses for them are calculated/simulated in the right column according to the circuit parameters from TABLE 3.

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Maximum Voltage Stress</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>$V_{st_1_{max}} + V_o \times \frac{N_{pri}}{N_{sec}}$</td>
<td>350V</td>
</tr>
<tr>
<td>D1</td>
<td>$V_{st_1_{max}} \times \frac{N_{sec}}{N_{pri}} + V_o$</td>
<td>117V</td>
</tr>
<tr>
<td>Q2</td>
<td>$V_o \times \frac{N_{buf}}{N_{sec}} - V_{sto_{min}}$</td>
<td>130V</td>
</tr>
<tr>
<td>D2</td>
<td>$\max \left[ V_{st_{1_{max}}}(t) \times \frac{N_{buf}}{N_{sec}} + V_o(t) \right]$</td>
<td>310V</td>
</tr>
<tr>
<td>D3</td>
<td>$\max \left[ V_{st_{1_{min}}}(t) - V_{st_{max}}(t) \right]$</td>
<td>150V</td>
</tr>
<tr>
<td>Q3</td>
<td>$\max \left[ V_{st_{1_{max}}}(t) - V_{st_{max}}(t) \right]$</td>
<td>10V</td>
</tr>
</tbody>
</table>

#### B. Component Current Stress

The switching current in Q1 peaks at $t_2$ when $P_{in} < P_{LED}$. It is equal to $I_{pri_{req}}$ that is generated by the feedback loop. The switching current in Q1 peaks two times at $t_1$ and $t_3$, respectively, when $P_{in} > P_{LED}$. The peak current at $t_1$ is also equal to $I_{pri_{req}}$ while smaller at $t_3$ except, when $P_{in} = 2P_{LED}$, the peak current at $t_1$ and $t_3$ are equal. Therefore, the maximum current stress of $D_1$ is calculated to be $3A$. The maximum current in $D_2$ and $Q_3$ is calculated to be $1A$.

The maximum current with $D_1$ can be expressed as:

$$I_{D1_{max}} = I_{sec_{pk}} = I_{pri_{req}} \times \frac{N_{pri}}{N_{sec}}$$

Eq. (17) describes the relationship between $I_{pri_{req}}$ and $I_{LED}$. Once the circuit parameters, $I_{LED}$, $V_o$, $T_s$, and $I_{pri_{req}}$ are determined, $I_{pri_{req}}$ can be calculated. $I_{pri_{req}}$ is calculated to be 1A at 15W output power with the circuit parameter from TABLE 3. The maximum current stress with $D_1$ can be expressed as:

$$I_{D1_{max}} = I_{sec_{pk}} = I_{pri_{req}} \times \frac{N_{pri}}{N_{sec}}$$

C. Storage Capacitor Requirement

The high voltage film capacitor $C_{sto}$ is used to buffer the imbalanced energy in a half line cycle. The value of $C_{sto}$ is determined by the amount of imbalanced energy and the designed voltage range for $V_{sto}$. The relationship among the imbalanced energy, $E_{buffer}$, the minimum voltage of $V_{sto}$, and the maximum voltage of $V_{sto}$ can be expressed as:

$$E_{buffer} = \frac{1}{2} C_{sto} \times (V_{sto_{max}}^2 - V_{sto_{min}}^2)$$

Where

$$V_{sto_{avg}} = \frac{V_{sto_{max}} + V_{sto_{min}}}{2}$$

And

$$V_{sto_{pp_{rip}}} = V_{sto_{max}} - V_{sto_{min}}$$

$V_{sto_{avg}}$ represents the average voltage of $V_{sto}$ and $V_{sto_{pp_{rip}}}$ represents the double-line-frequency peak to peak ripple voltage of $V_{sto}$. Rearranging Eq. (22) yields:

$$C_{sto} = \frac{E_{imbalance}}{V_{sto_{avg}} \times V_{sto_{pp_{rip}}}}$$

At the same time, $E_{buffer}$ can also be expressed as:

$$E_{buffer} = \frac{1}{2} \times P_{LED} \times \frac{1}{2} \times T_{line}$$

Combining Eq. (23) and (24) yields:

$$C_{sto} = \frac{P_{LED} \times T_{line}}{2 \pi \times V_{sto_{avg}} \times V_{sto_{pp_{rip}}}}$$

Eq. (25) reveals that the capacitance of $C_{sto}$ is inversely proportional to the average voltage $V_{sto_{avg}}$ and the peak to peak ripple amplitude $V_{sto_{pp_{rip}}}$. When a higher average voltage $V_{sto_{avg}}$ and / or a larger ripple amplitude $V_{sto_{pp_{rip}}}$ is designed in the proposed LED driver, $C_{sto}$ can be reduced to achieve...
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TABLE 2 STORAGE CAPACITOR REQUIREMENT COMPARISON BETWEEN DIFFERENT LED DRIVING SOLUTIONS

<table>
<thead>
<tr>
<th>Topology</th>
<th>Storage Capacitor Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-stage Flyback LED driver</td>
<td>Voltage rating: can be decided based on the LED voltage</td>
</tr>
<tr>
<td></td>
<td>Capacitance: High. Determined by the requirement of flicker level. Electrolytic capacitors are required to implement the storage capacitor.</td>
</tr>
<tr>
<td></td>
<td>Example: 1mF electrolytic capacitors are used on a 12W, 41V LED driver [30]. The normalized capacitance per wattage is 83μF/W.</td>
</tr>
<tr>
<td>Two-stage Flyback + Buck LED driver</td>
<td>Voltage rating: can be decided based on LED voltage. The bus voltage is usually designed to be the LED voltage plus a reasonable voltage margin for proper Buck converter operation. For example, 63V voltage rated capacitors can be used when the maximum LED voltage is 50V.</td>
</tr>
<tr>
<td></td>
<td>Capacitance: High. Determined by the acceptable bus voltage ripple. Usually implemented by electrolytic capacitors.</td>
</tr>
<tr>
<td></td>
<td>Example: 1mF, 63V, electrolytic capacitors are used in a 30W, 45V, two-stage LED driver design [31]. The normalized capacitance per wattage is 33μF/W.</td>
</tr>
<tr>
<td>Proposed cycle by cycle energy buffering LED driver</td>
<td>Voltage rating: High. The storage capacitors are biased at high voltage (usually 100V to 300V voltage) and allow a high peak to peak double line frequency voltage ripple. The voltage rating of the storage capacitor is not linked to the LED voltage.</td>
</tr>
<tr>
<td></td>
<td>Capacitance: Low. A few microfarads to enable film capacitor implementation. Eq.(25) can be used to calculate the required capacitor.</td>
</tr>
<tr>
<td></td>
<td>Example: 2 x 3.3μF, 300V film capacitors are used in the proposed LED driver. The normalized capacitance per wattage is 0.44μF/W in the proposed design.</td>
</tr>
<tr>
<td>Previous active filter LED driver</td>
<td>The rule to select the storage capacitor is the same as the proposed LED driver.</td>
</tr>
</tbody>
</table>

(b) gate driving logic when \( P_{in} < P_{LED} \), (c) gate driving logic when \( P_{in} > P_{LED} \), (d) operation flow of the proposed LED driver in a switching cycle

electrolytic capacitor-free design. The energy storage capacitors requirement of the proposed LED driver will be compared to the requirement of other LED driving technologies and the result is summarized in TABLE 2.

IV. CONTROL STRATEGY

Fig. 13 (a) shows the control diagram of the proposed energy buffering LED driver and Fig. 13(b) & (c) give the example gate driving logic for both \( P_{in} > P_{LED} \) and \( P_{in} < P_{LED} \). There are two control loops, LED current loop and Vsto voltage loop in the system.

In the Vsto voltage loop, the averaged voltage of Vsto, \( V_{sto\_avg} \), is compared with its reference, \( V_{sto\_ref} \). The compensated error, \( V_{comp} \), multiplies the scaled input voltage, \( V_{in\_req\_is} \), and the result becomes the reference of the AC input current. The average input current is obtained by taking \( I_{pri\_sns} \), which corresponds to (t3-t2) in Fig. 8 and (t'2-t'1) in Fig. 10, can be described by (18). The secondary side current conduction time, \( T_{dis} \), is 83μF/W.

\[ T_{dis} = \frac{I_{sec\_pk} \times T_{dis}}{2 \times T_{i}} \]  

(26)

Where \( T_{dis} \) is equal to \( (t_2-t_1) \) in Fig. 8 and \( (t'_2-t'_1) \) in Fig. 10. Combining Eq. (18) and (26) yields:

\[ I_{LED} = \frac{I_{LED\_req\_pri} \times T_{dis} \times N_{pri}}{2 \times T_{i} \times N_{sec}} \]  

(27)

It is worth mentioning that the proposed LED driving method enables primary side current regulation. Under steady state, the peak secondary side current in every switching cycle is described by (18). The secondary side current conduction time, which corresponds to \((t_1-t_2)\) in Fig. 8 and \((t'_1-t'_2)\) in Fig. 10, can be sensed by detecting winding voltages. Therefore, the averaged secondary side current in one switching cycle can be expressed as:

\[ I_{LED} = \frac{I_{sec\_pk} \times T_{dis}}{2 \times T_{i}} \]  

Where \( T_{dis} \) is equal to \((t_2-t_1)\) in Fig. 8 and \((t'_2-t'_1)\) in Fig. 10. Combining Eq. (18) and (26) yields:

\[ I_{LED} = \frac{I_{LED\_req\_pri} \times T_{dis} \times N_{pri}}{2 \times T_{i} \times N_{sec}} \]  

(27)
Once $I_{\text{pri req}}$ and $T_{\text{dis}}$ are available, the LED current can be estimated without additional sensing on the secondary side. [28] and [29] have the details of primary side circuit sensing technology and will not be further discussed in this paper.

Fig. 14 illustrates the high level power flow of the proposed cycle by cycle energy buffering LED driver. When $P_{\text{in}} < P_{\text{LED}}$, the storage capacitor will supply the amount of power, $P_{\text{LED}} - P_{\text{in}}$, to the LED load. When $P_{\text{in}} > P_{\text{LED}}$, the extra power from the AC input, $P_{\text{in}} - P_{\text{LED}}$, will be directed to be stored in the storage capacitor.

![Fig. 14 Power flow of the proposed cycle by cycle energy buffering LED driver](image_url)

**V. LOSS ANALYSIS**

In this section, a loss analysis of the proposed cycle by cycle energy buffering LED driver, as well as the previous active filtering, LED driver will be performed. To fairly compare the losses from both designs, the parameters of MOSFETs and diodes used in the analysis are standardized. In this way, the analysis has a much less dependence on the components parameter, and the result can strongly reflect the advantages/disadvantages of each design from the perspective of power circuit topology and operation condition. For the proposed cycle by cycle energy buffering LED driver, the following losses had been identified.

For MOSFET Q1, under both $P_{\text{in}} < P_{\text{LED}}$ and $P_{\text{in}} > P_{\text{LED}}$ operating condition, there are conduction loss during $[t_0-t_1]$, output capacitor switching loss at $t_1$. When $P_{\text{in}} < P_{\text{LED}}$, there is turn off overlap switching loss at $t_1$. When $P_{\text{in}} > P_{\text{LED}}$, there is turn off overlap switching loss at $t_1$ and $t_2$.

For MOSFET Q2, there is only conduction loss during $[t_3-t_4]$ when $P_{\text{in}} > P_{\text{LED}}$. One should note that the body diode of Q2 is forward biased before it is turned on. Therefore, there is no turn on overlap switching loss and output capacitor switching loss. There is no turn off switching loss with Q2 as well since the switching current in it is already zero before Q2 is turned off.

For MOSFET Q3, there is turn on overlap switching loss and output capacitor switching loss at $t_1$ when $P_{\text{in}} < P_{\text{LED}}$. There is no turn off switching loss with Q3 since its switching current is already zero before Q3 is turned off (turn off Q1 at $t_2$ terminates the switching current).

For diode D1, there are conduction losses during $[t_2-t_3]$ when $P_{\text{in}} < P_{\text{LED}}$ and during $[t_1-t_2]$ when $P_{\text{in}} > P_{\text{LED}}$.

For diode D2, there is conduction loss during $[t_3-t_4]$ when $P_{\text{in}} > P_{\text{LED}}$.

For diode D3, there is conduction loss during $[t_1-t_2]$ when $P_{\text{in}} < P_{\text{LED}}$.

There are also losses from the equivalent lump leakage inductance at the primary side. The leakage inductance, between the primary side main winding and the secondary side main winding, is estimated to be 4% of the primary side main winding inductance, due to relatively poor coupling caused by galvanic isolation. The leakage inductance, between the primary side main winding and the buffering winding, is estimated to be 2% of the primary side main winding inductance as galvanic isolation is not required and good coupling can be achieved. When $P_{\text{in}} < P_{\text{LED}}$, there is energy built up in the leakage inductor as the primary side switching current grows during $[t_0-t_1]$. When $P_{\text{in}} > P_{\text{LED}}$, there is energy build up in the leakage inductor as the primary side switching grows during $[t_0-t_1]$ and $[t_0-t_1]$, respectively. These energies are dissipated in a snubber circuit as loss.

For the Flyback transformer, there is core and copper loss. A detailed estimation of this loss requires very complex analysis, however, with a reasonably good design, the total loss from the transformer is estimated to be 2% of the power it will handle.

The detailed loss breakdown of the proposed cycle by cycle energy buffering LED driver is shown in TABLE 4 in the appendix as well as presented in bar chart below.

Also, the detailed loss breakdown for the previous active filter LED driver is performed, and the result is shown in TABLE 5 as well as the bar chart in Fig. 15 and Fig. 16 below.

![Fig. 15 Loss breakdown of the proposed cycle by cycle energy buffering LED driver](image_url)

![Fig. 2 Loss breakdown of the previous active filtering LED driver](image_url)

To estimate the power losses from the Buck (release imbalanced energy) and Boost (store imbalanced energy) converters in the previous active filtering LED driver, the following assumption is made.

1. The switching frequency of the Buck and Boost converters is also 25kHz, which benchmarks the switching frequency of the proposed LED driver.

2. The inductor used in the Buck and Boost converter is 1.2mH, which is equal to the inductance value of the primary side winding of the Flyback transformer in the proposed LED driver. In this way, the magnetic components used in both designs are at a comparable level and can be assumed to have the same level of power loss.
The total loss generated by the proposed cycle by cycle energy buffering LED driver and the previous active filtering LED driver are calculated/estimated to be 1815mW and 2006mW, respectively for 15W output power. It should note that the majority of losses, in both designs, are from diode conduction loss, leakage inductance loss, transformer loss. Because of low frequency (25kHz) operation, the related switching loss is not significant. In addition to the quantitative analysis on the loss breakdown, the loss difference between these two designs can also be understood from the perspective of energy process steps.

The proposed LED driver requires one less power conversion step with the imbalanced energy.

Also because of noise, mis-triggers occur and results in several current has a small level of variation in the measured waveform. The above steps provide an example procedure to design the proposed LED driver. Like any other designs, it can always start the design procedure in a different order. For example, one can set the maximum voltage stresses and current stresses of components in the beginning and then design other parameters that around this objective.

VII. SIMULATION AND EXPERIMENTAL RESULT

To verify the operating principle of the proposed LED driver, a 15W simulation model and experimental prototype had been built, simulated, and tested. The circuit parameter is shown in TABLE 3.

![Fig. 18 shows the simulated secondary side switching current waveforms. A rather flat peak primary side switching current is shown in the simulated result, which completely agrees with the analysis. Due to sensing circuit limitation and delay, the measured primary side peak switching current has a small level of variation in the measured waveform. Also because of noise, mis-triggers occur and results in several spikes and dips scattered in a half line cycle period.](image)

![Fig. 18 shows the simulated secondary side switching current and the LED current at line frequency time scale. The peak secondary side switching current is a constant in a half line cycle. Therefore, the averaged secondary side current, which is also equal to the LED current, is a constant in a half line cycle and flicker-free LED driving performance is achieved.](image)
Fig. 17 Primary side switching current, (a) simulated result (PSIM 11.0), (b) measured waveform

Fig. 18 Simulated key waveforms at line cycle time scale (PSIM 11.0)

Fig. 19 Simulated key switching waveforms when $P_{in} < P_{LED}$ (PSIM 11.0)

Fig. 3 Key switching waveforms when $P_{in} < P_{LED}$

Fig. 4 Simulated key switching waveforms when $P_{in} > P_{LED}$ (PSIM 11.0)

Fig. 22 Key switching waveforms when $P_{in} > P_{LED}$

Fig. 23 shows the key waveforms of line frequency operation, which includes the AC input current, the LED voltage, the LED current and the storage capacitor voltage $V_{sto}$. The LED voltage is almost a constant. FFT function is used to measure 120Hz ripple LED current to avoid misreading due to switching noise. The RMS ripple LED current at 120Hz is 10.67mA,

by LED output. $Q_1$ is turned off to end the primary side switching current and the magnetic current commutes to the secondary side winding. During $[t_1-t_2]$, the magnetic current flows in the secondary side winding and delivered to the LED load. The secondary side current drops to zero at $t_2$ and $Q_1$ is turned on again. The MOSFET $Q_2$ is also turned on at $t_2$. During $[t_2-t_3]$, more current is drawn from the AC input. At $t_3$, the total current drawn from AC input reaches the level required by performing power factor correction and $Q_1$ is turned off again. The magnetic current commutes from the primary side winding to the buffer winding. The extra energy in the transformer is then transferred to the capacitor $C_{sto}$. The MOSFET $Q_1$ is always off during this operation condition. Fig. 22 shows the measured waveforms and it highly agrees with simulated result.
which corresponds to 15mA peak ripple and is 6% of the average LED current. The voltage on the storage capacitor, $V_{sto}$, changes from 120V as the minimum to 170V as the maximum in a half line cycle, to buffer the imbalanced energy. It is worth mentioning that, due to sensing circuit limitation, the peak of the switching current $I_{pri}$ varies a bit in a half line cycle, which results in a less than ideal output current waveform. A better output current waveform can be achieved with an improved sensing circuit design; the simulation waveform in Fig. 18 verifies that.

Fig. 23 Key waveforms in double line frequency operation

Fig. 24 compares the efficiency of the proposed LED driver and a comparable conventional single-stage LED driver. At full load, the efficiency of the proposed LED driver is 1.9% lower than the efficiency of a conventional Flyback LED driver, which is a very small price to pay when flicker-free and electrolytic capacitor free operation have been achieved.

Fig. 24 Efficiency comparison between the proposed LED driver and a conventional LED driver under 110Vrms input

Fig. 25 shows the power factor of the proposed LED driver. At full load, the experimental prototype achieves 0.94PF, which meets the requirement from EnergyStar.

VIII. CONCLUSION

Eliminating electrolytic capacitors in LED driver designs is critical to extending the lifetime of LED lighting fixtures. An alternative three-port LED driver - cycle by cycle energy buffering LED driver has been proposed in the paper to achieve electrolytic-less and flicker-free operation. By directly controlling the switching current, the following improvements are made with the proposed LED driver over previous three-port LED drivers. First, the imbalanced energy in a half line cycle experiences one less power conversion step, which reduces conversion loss and improves overall efficiency. Second, the maximum energy that needs to be stored in the transformer in the proposed design is half the amount of conventional and other electrolytic capacitor-less designs, which allows the use of a smaller magnetic core. Third, primary side current regulation can be easily implemented, which can reduce design complexity on controller circuit. A potential integrated primary side controller can be implemented based on this method. A 15W experimental prototype had been built and tested to verify the operating principle. 0.94PF has been achieved and each order of harmonic currents are measured, and they are all below the limit from IEC-61000-3-2. The efficiency of the proposed LED driver is only 1.9% lower than a conventional single-stage LED driver at full load, which is a low price to pay when achieving flicker-free operation and electrolytic capacitor-less design. Two 3.3µF film capacitor have been used in the prototype to buffer double-line-frequency imbalanced energy. The 120Hz ripple current is measured to be 6% of the average LED current. Overall, the experimental result demonstrates a very good LED driving performance compared
with existing options, and a high degree of agreement with the analysis presented.

**APPENDIX**

For MOSFET, the following parameters are used in the loss calculation.

- **CQoss**: MOSFET parasitic output capacitance 13pF
- **RQon**: On resistance of MOSFET 1.4 ohm
- **TQr**: MOSFET turn on rise time 15ns
- **TQf**: MOSFET Turn off fall time 15ns

For diode, the following parameter is used in the loss calculation.

- **VD_F**: Diode forward voltage drop 1.5V

The switching frequency is 25kHz. The loss breakdown of the proposed cycle by cycle energy buffering LED driver and the previous active filtering LED driver are shown in TABLE 4 and TABLE 5.

### TABLE 4. LOSS BREAKDOWN OF THE PROPOSED CYCLE BY CYCLE ENERGY BUFFERING LED DRIVER

<table>
<thead>
<tr>
<th>Calculation formula</th>
<th>Result (mW)</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_{cond} ( \equiv \frac{1}{2} I_{rms} \times R_{Q,on} )</td>
<td>134</td>
<td>( P_{Q1, cond} ): Conduction loss of Q1, ( I_{rms} ): RMS current in Q1, 0.32A</td>
</tr>
<tr>
<td>( P_{Q1, oas} )</td>
<td>-0</td>
<td>( P_{Q1, oas} ): Output capacitor switching loss of Q1 when ( P_{in} &lt; P_{LED} ), ( V_{Q1, ds, on} ): Drain to source voltage of Q1 before turn on when ( P_{in} &lt; P_{LED} ), (-60V) (average)</td>
</tr>
<tr>
<td>( P_{Q1, on} )</td>
<td>20.6</td>
<td>( P_{Q1, on} ): MOSFET turn on switching loss when ( P_{in} &lt; P_{LED} ), ( I_{Q1, pk1} ): Peak switching current in Q1 when ( P_{in} &lt; P_{LED} ), 1A, ( I_{Q1, pk2} ): Drain to source voltage of Q1 after turning off when ( P_{in} &lt; P_{LED} ), (-320V)</td>
</tr>
<tr>
<td>( P_{Q1, peak} )</td>
<td>-0</td>
<td>( V_{Q1, ds, off1} ): Drain to source voltage of Q1 before turn on when ( P_{in} &gt; P_{LED} ), (-130V)</td>
</tr>
<tr>
<td>( P_{Q1, off} )</td>
<td>6.1</td>
<td>( P_{Q1, off} ): 1st turn off overlap switching loss of Q1 when ( P_{in} &gt; P_{LED} ), ( I_{Q1, pk1} ): Peak switching current in Q1 when ( P_{in} &gt; P_{LED} ), (-280V), ( I_{Q1, pk2} ): 2nd peak switching current in Q1 when ( P_{in} &gt; P_{LED} ), 1A</td>
</tr>
<tr>
<td>( P_{Q1, off} )</td>
<td>4.3</td>
<td>( P_{Q1, off} ): 2nd turn off overlap switching loss of Q1 when ( P_{in} &gt; P_{LED} ), ( I_{Q1, pk1} ): Peak switching current in Q1 when ( P_{in} &gt; P_{LED} ), (-130V) (peak switching current changes from 0A to 1A)</td>
</tr>
<tr>
<td>( P_{D1, con} )</td>
<td>375</td>
<td>( P_{D1, con} ): Diode conduction loss, ( I_{rms} ): Average current in D1, 0.25A</td>
</tr>
<tr>
<td>( P_{D1, oas} )</td>
<td>30</td>
<td>( P_{D1, oas} ): Conduction loss of D2, ( I_{rms} ): RMS current in Q1, 0.15A</td>
</tr>
<tr>
<td>( P_{D1, con} )</td>
<td>55</td>
<td>( P_{D1, con} ): Q2 conduction loss, ( I_{rms} ): RMS current in Q2, 0.04A</td>
</tr>
<tr>
<td>( P_{Q1, on} )</td>
<td>8.8</td>
<td>( P_{Q1, on} ): Turn on overlap switching loss with Q1, ( V_{Q1, ds, on} ): Drain to source voltage of Q1 before turn on (-70V), ( I_{Q1, pk} ): Peak switching current in Q1, 0.17A</td>
</tr>
<tr>
<td>( P_{Q3, con} )</td>
<td>39</td>
<td>( P_{Q3, con} ): Conduction loss of D3, ( I_{rms} ): RMS current in Q3, 0.16A</td>
</tr>
<tr>
<td>( P_{Q3, oas} )</td>
<td>52</td>
<td>( P_{Q3, oas} ): Conduction loss of D3, ( I_{rms} ): RMS current in Q3, 0.04A</td>
</tr>
<tr>
<td>( P_{Q3, oas} )</td>
<td>0.3</td>
<td>( P_{Q3, oas} ): Q3 output capacitor switching loss</td>
</tr>
<tr>
<td>( P_{L1} )</td>
<td>300</td>
<td>( P_{L1} ): Leakage inductor loss when ( P_{in} &lt; P_{LED} ), ( L_{1, max} ): Estimated leakage inductance between the primary side main winding and the second side main winding, 4% * ( L_{1max} )= 48µF</td>
</tr>
<tr>
<td>( P_{L2} )</td>
<td>300</td>
<td>( P_{L2} ): Leakage inductor loss generated by the first primary pulse current when ( P_{in} &lt; P_{LED} ), ( L_{2, max} ): Estimated leakage inductance between the primary side main winding and the second side main winding, 24µF</td>
</tr>
<tr>
<td>( P_{L3} )</td>
<td>75</td>
<td>( P_{L3} ): Leakage inductor loss generated by the second primary pulse current when ( P_{in} &lt; P_{LED} ), ( L_{3, max} ): Leakage inductance between the primary side main winding and the buffer winding, 48µF</td>
</tr>
<tr>
<td>( P_{max, est} )</td>
<td>395</td>
<td>( P_{max, est} ): Estimated sum of core and copper losses of the Flyback transformer, ( 2% * P_{LED} )= 0.3W</td>
</tr>
<tr>
<td>Total</td>
<td>1815</td>
<td></td>
</tr>
</tbody>
</table>
### TABLE 5 LOSS BREAKDOWN OF PREVIOUS ACTIVE FILTERING LED DRIVER

<table>
<thead>
<tr>
<th>Calculation formula</th>
<th>Result (mW)</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{\text{cond}} )</td>
<td>( I_{\text{Q1, on}} \times R_{\text{Q1, on}} )</td>
<td>134</td>
</tr>
<tr>
<td>( P_{\text{cap}} )</td>
<td>( \frac{1}{4} C_{\text{Q1, on}} \times V_{\text{Q1, on}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>1</td>
</tr>
<tr>
<td>( P_{\text{off}} )</td>
<td>( \frac{1}{2} \times V_{\text{Q1, off}} \times T_{\text{Q1, off}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>13</td>
</tr>
<tr>
<td>( P_{\text{cond}} )</td>
<td>( I_{\text{D1, avg}} \times V_{\text{D1, f}} )</td>
<td>375</td>
</tr>
<tr>
<td>( P_{\text{L}} )</td>
<td>( \frac{1}{2} P_{\text{inductor}} \times L_{\text{inductor}} \times 2 T_{\text{Q1, off}} )</td>
<td>600</td>
</tr>
<tr>
<td>( P_{\text{L}} )</td>
<td>( P_{\text{inductor}} \times 2 )</td>
<td>300</td>
</tr>
<tr>
<td>( P_{\text{Q1, on}} )</td>
<td>( I_{\text{Q1, on}} \times V_{\text{Q1, on}} \times f_{\text{slew}} \times 2 T_{\text{Q1, off}} )</td>
<td>49</td>
</tr>
<tr>
<td>( P_{\text{Q1, off}} )</td>
<td>( \frac{1}{2} V_{\text{Q1, off}} \times T_{\text{Q1, off}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>7.7</td>
</tr>
<tr>
<td>( P_{\text{Q1, cap}} )</td>
<td>( \frac{1}{2} C_{\text{Q1, on}} \times V_{\text{Q1, on}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>1.6</td>
</tr>
<tr>
<td>( P_{\text{Q1, cond}} )</td>
<td>( I_{\text{D1, avg}} \times V_{\text{D1, f}} )</td>
<td>138</td>
</tr>
<tr>
<td>( P_{\text{Q1, off}} )</td>
<td>( \frac{1}{2} V_{\text{Q1, off}} \times T_{\text{Q1, off}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>3.3</td>
</tr>
<tr>
<td>( P_{\text{Q1, cap}} )</td>
<td>( \frac{1}{2} C_{\text{Q1, on}} \times V_{\text{Q1, on}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>0.3</td>
</tr>
<tr>
<td>( P_{\text{Q1, cond}} )</td>
<td>( I_{\text{D1, avg}} \times V_{\text{D1, f}} )</td>
<td>102</td>
</tr>
<tr>
<td>( P_{\text{Q1, off}} )</td>
<td>( \frac{1}{2} V_{\text{Q1, off}} \times T_{\text{Q1, off}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>95.5</td>
</tr>
<tr>
<td>( P_{\text{Q1, cap}} )</td>
<td>( \frac{1}{2} C_{\text{Q1, on}} \times V_{\text{Q1, on}} \times f_{\text{slew}} \times 2 T_{\text{Q1, on}} \times T_{\text{Q1, off}} )</td>
<td>95.5</td>
</tr>
<tr>
<td>( P_{\text{cond}} )</td>
<td>( I_{\text{D1, avg}} \times V_{\text{D1, f}} )</td>
<td>102</td>
</tr>
<tr>
<td>( P_{\text{cond}} )</td>
<td>( I_{\text{D1, avg}} \times V_{\text{D1, f}} )</td>
<td>102</td>
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</table>
REFERENCES


Bo Sheng (S’17) received his M.S degree from the Department of Electrical and Computer Engineering, Shanghai University of Electric Power, in 2016. He is working toward his Ph.D. degree at Queen’s university. His areas of interest include high efficiency resonant DC/DC converters.

Samuel Webb (S’17) received his B.S degree from the Department of Electrical and Computer Engineering, Queen’ university, Canada, in 2016. He is working toward his Ph.D. degree in the same university. His areas of interest include extremely high efficiency DC/DC converters for point-of-load applications.

ZHANG Yan received the Ph.D. degree in the major of Electrical Engineering from Xi’an Jiaotong University (XJTU), Xi’an, China, in 2014. Then he has been working as a teaching faculty, and he is currently an associate professor in the school of Electrical Engineering in XJTU. From early 2016 to 2017, he was a Postdoctoral Research Fellow in the Department of Electrical and Computer Engineering, Queen’s University, Kingston, ON, Canada. His research interests include topology, model and control of power electronic systems, high efficiency resonant dc-dc converters, and power-electronics applications in renewable energy and distributed generation. Dr. ZHANG has presided over research projects includes National Natural Science Foundation, China Postdoctoral Science and Province Foundation, Power Electronics Science and Education Development Program of Delta Environmental & Educational Foundation, State key lab Foundation. He has published more than 30 papers technical papers in peer-reviewed journals and conference proceedings and holds 4 China issued invention patents.

Yan-Fei Liu (M’94–SM’97-F’13) received his Bachelor and Master’s degree from the Department of Electrical Engineering from Zhejiang University, China, in 1984 and 1987 and PhD degree from the Department of Electrical and Computer Engineering, Queen’s University, Kingston, ON, Canada, in 1994. He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, in Ottawa, Canada from 1994 to 1999. Since 1999, he has been with Queen’s University, where he is currently a Professor with the Department of Electrical and Computer Engineering. His current research interests include digital control technologies for high efficiency, fast dynamic response dc–dc switching converter and ac–dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He has authored over 230 technical papers in the IEEE Transactions and conferences and holds 25 U.S. patents. He is also a Principal Contributor for two IEEE standards. He is a Fellow of Canadian Academy of Engineering and received Modeling and Control Achievement Awards from IEEE Power Electronics Society. He received Premier’s Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997.