A High Frequency Dual-Channel Isolated Resonant Gate Driver with Low Gate Drive Loss for ZVS Full-Bridge Converters

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\textbf{Abstract} – As switching frequency increases, to reduce the gate drive loss combined with the Zero-Voltage-Switching (ZVS) technique is meaningful for the widely used Full-Bridge (FB) converters. A dual-channel isolated Resonant Gate Driver (RGD) is proposed in this paper. The proposed RGD is able to provide two isolated complementary drive signals for a pair of power MOSFETs in one bridge leg. Furthermore, the proposed RGD reduces about 79 \% gate drive loss compared to the conventional Voltage Source Driver (VSD). In addition, the negative gate drive voltage provided by the proposed RGD prevents the false trigger problem in the FB converters. The comparison to the conventional VSDs demonstrates the power loss reduction achieved by the proposed RGD. The principle of operation and optimum design of the proposed RGD are given in detail. A 200-VDC input, 48-V/ 20-A output and 500-kHz phase-shift ZVS FB converter with the proposed RGD was built to verify the advantages and efficiency improvement.

\textbf{Index Terms}: Resonant Gate Driver (RGD), power MOSFET, Zero-Voltage Switching (ZVS), Full-Bridge (FB)

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I. INTRODUCTION

To increase the switching frequency of the power converters can help to reduce the size and volume of the passive components, such as the inductors, transformers, and capacitors, so that the power density can be increased. However, as the switching frequency increases, the switching loss and gate drive loss increase proportionally [1]-[3]. In recent years, a lot of work has been done to reduce, or eliminate the switching loss. Soft switching technique is one of the effective solutions to reduce the switching loss at high switching frequency. With Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS), the Full-Bridge (FB) converters exhibit lower switching loss and are widely used in many applications [4]-[7]. However, the excessive gate drive loss may still exist and cause lower efficiency and reliability as the switching frequency increases.

In the last twenty years, Resonant Gate Drivers (RGDs) have been proposed with the objective of recovering gate energy loss in the conventional Voltage Source Drivers (VSDs) [8]-[11]. The basic idea of the RGDs is to utilize the L-C resonance to recover the gate drive energy stored in the gate capacitance of the power MOSFET. The review on the RGD topologies concentrating on gate energy recovery efficiency has been reported in [12]-[13]. The general circuit model and design method of the RGDs are proposed in [14]. A high-speed RGD with controlled peak gate voltage is proposed for the Silicon Carbide (SiC) MOSFETs in [15]. An assessment of the RGD techniques for use in low power dc/dc converters is presented in [16] and the mathematical model is built to estimate the power loss of the drive circuit in [17]. However, there was little work reported on the RGDs suitable for the FB converters to reduce the excessive gate drive loss with the ZVS technique at high switching frequency.

Most of the reported RGDs can be classified into three categories when applied to a ZVS FB converter.

1) The RGDs designed for one single power MOSFET [18]-[24]. To drive a FB converter, four sets of these RGDs are needed, which increases the complexity and cost significantly. The RGDs in [22]-[24] can provide the negative gate drive voltage to prevent the false trigger problem caused by fast $dv/dt$ during the turn-off transition. Though the RGD in [22] can provide the negative gate drive voltage, the amplitude of the...
gate-to-source voltage is affected by the resonant components seriously. Compared to [23], the RGD proposed in [24] is more concise and can recover more gate drive energy.

2) The RGDs designed for two ground-sharing power MOSFETs [25]-[26]. Basically, these RGDs are only able to drive two power MOSFETs sharing the same ground and not applicable to the power MOSFETs in one bridge leg. These RGDs are not suitable for the FB converter with the floating ground.

3) The RGDs designed for two power MOSFETs in one bridge leg [27]-[29]. These RGDs can reduce the complexity of the drive circuits in the FB converters. However, the level-shift circuit in the RGD is prone to noise and may lead to the shoot-through problem in the FB converter [27]. In [28], the power MOSFET gate terminal is not actively clamped high or low, which results in lower noise immunity. In [29], the resonant inductor of the RGD suffers the input voltage. When the input voltage becomes high, the resonant inductance should have to increase significantly, which is not suitable for the FB converters. Furthermore, this type of the RGDs can not provide the negative gate drive voltage to prevent the false trigger in the FB converters.

Based on the above analysis, the desired RGD for a FB converter should have the following characteristics: 1) recover the gate drive energy with high efficiency; 2) is able to drive two power MOSFETs in one bridge leg as dual channel drivers with low components count and low cost; 3) provide the negative gate drive voltage to prevent the false trigger with high reliability.

The objective of the paper is to propose a dual-channel isolated RGD solution suitable for the FB converters with the above advantages. The proposed RGD is able to drive two MOSFETs in one bridge-leg with the controlled dead time, which leads to the simplicity and low cost. The negative gate drive voltage ensures high reliability of the turn-off status to avoid fast $dv/dt$ problem over the previously proposed RGDs. These benefits make the proposed one suitable for the FB converters. Section II presents the review of the gate drive circuits. Section III presents the proposed isolated RGD and its principle of operation. Section IV is the loss analysis and the optimal design for the proposed RGD. Section V gives the comparison between the proposed RGD and previous gate drive circuits. The simulation results are also provided in Section VI. Section VII contains the experimental results and discussion. Section VIII is the conclusion.
II. REVIEW OF GATE DRIVE CIRCUITS

A. The Conventional Voltage Source Drivers for the FB Converters

Fig. 1 shows the conventional Voltage Source Driver (VSD) in the FB configuration for a single power MOSFET. In this circuit, $S_1$-$S_4$ are the drive switches, $R_{\text{ext}}$ is the external resistance, $R_g$ is the gate mesh resistance, $C_{g,Q}$ represents the input capacitance of the power MOSFET $Q$, $i_g$ is the gate current, and $v_{gs}$ is the gate-to-source voltage. When $S_1$ and $S_4$ are on, $v_{gs}$ is equal to $V_c$ and the power MOSFET $Q$ is on. When $S_2$ and $S_3$ are on, $v_{gs}$ is equal to $-V_c$ and $Q$ is off. However, during the turn-off transition, the electric charge $2C_{g,Q}V_c^2$ provided by the dc power supply is completely dissipated in the resistors $R_{\text{ext}}$ and $R_g$. Furthermore, as the switching frequency increases, the drive power consumption increases proportionally.

![Fig. 1 The conventional VSD for a single MOSFET](image)

For the FB converters, the conventional transformer coupled VSD shown in Fig. 2 is widely used. $S_1$-$S_4$ are the drive switches, $D_1$-$D_4$ are the freewheel diodes, $R_{\text{ext1}}$ and $R_{\text{ext2}}$ are the external resistors, $R_{g1}$ and $R_{g2}$ are the gate mesh resistance. This VSD has the ability to drive two power MOSFETs in one bridge leg with isolation, leading to the low complexity and high reliability. Unfortunately, in this VSD, the energy provided to drive the power MOSFETs still dissipates totally in the resistors $R_{g1}$, $R_{\text{ext1}}$, $R_{g2}$, and $R_{\text{ext2}}$.

![Fig. 2 The transformer coupled VSD for two MOSFETs in one bridge leg](image)
B. Candidates of the RGDs for the FB Converters

Most of the reported RGD topologies are for non-isolated application. However, the FB converters require isolated gate drivers. Among these topologies, the RGDs proposed in [24] and [29] have respective advantages in the FB converter applications. It should be interesting to investigate these two RGDs particularly.

Fig. 3 shows the dual channel RGD proposed in [29]. In this circuit, $Q_1$ is the high side switch and $Q_2$ is the low side switch. The capacitance $C_2$ and diode $D_1$ forms a charge pump circuit. This dual channel RGD can recover more than $50\%$ of the conventional gate drive loss. However, the disadvantages of this RGD are as follows: 1) the input voltage is applied across the resonant inductance entirely. When the input voltage increases, the inductance has to be increased to guarantee the normal operation of the RGD. Therefore, this dual channel RGD is only suitable for the low voltage applications; 2) the dual channel RGD can not provide negative gate drive voltage, which may cause false trigger problem in the FB converters; 3) this dual channel RGD only provides two non-isolated drive signals, so it is not suitable to drive the Half-Bridge (HB) and FB converters in high power applications; 4) the current of the resonant inductance $L_r$ is continuous, which increases the conduction loss of the drive circuit itself.

On the other hand, the RGD in [24] can overcome the disadvantages of the dual channel RGD in [29], but this RGD has its own limitation when applied to the FB converters. Fig. 4 (a) shows the proposed RGD in [24]. $S_1$-$S_4$ are drive switches and $L_r$ is the resonant inductor. Fig. 4 (b) shows the equivalent circuit of the RGD in [24]. $C_{g,Q}$ represents the input capacitance of the power MOSFET $Q$. $v_g$ is the controllable voltage source decided by the drive switches $S_1$-$S_4$. This RGD utilizes the series L-C resonance to recycle the
electric charge stored in $C_{g,Q}$. However, it is designed for one single MOSFET. Each gate-driving circuit requires four drive switches ($S_1$-$S_4$) and an independent dc power supply (i.e. $V_c$). It should be noted that in one bridge leg, two MOSFETs do not share the same ground and therefore, two independent dc power supplies are required if this RGD is used. As a result, in a FB converter, two bridge legs require sixteen drive switches and four independent dc power supplies with many auxiliary components. This increases the complexity and cost significantly, and thus results in the low reliability. The further comparison between this RGD in [24] and the proposed dual-channel isolated RGD in this paper is given in Chapter IV.

The schematic and the equivalent circuit are shown in Fig. 4.

![Fig. 4 The RGD proposed in [24]](image)

III. PROPOSED RESONANT GATE DRIVER FOR FB CONVERTERS AND PRINCIPLE OF OPERATION

To overcome the drawbacks of the above circuits, the proposed isolated RGD is shown in Fig. 5. The circuit consists of four drive switches $S_1$-$S_4$, the drive transformer $T_r$, two resonant inductors $L_{r1}$ and $L_{r2}$. $L_{r1}$ and $L_{r2}$ can be the leakage inductance of the transformer. $Q_1$ is the high side switch and $Q_2$ is the low side switch in one bridge leg.

![Fig. 5 The proposed isolated RGD](image)
The gate waveforms of four drive switches, $S_1$-$S_4$, the voltage between $A$ and $B$, $u_{AB}$, the primary side current, $i_p$, along with the resonant inductor current, the gate-to-source voltage $v_{gs\_Q1}$, $v_{gs\_Q2}$ are illustrated in Fig. 6. $S_1$ and $S_2$, $S_3$ and $S_4$ are switched out of phase with the complementary control respectively. It is observed that the pulse width of $u_{AB}$ is controlled by the switching status of the four drive switches $S_1$-$S_4$. $i_{L1}$ and $i_{L2}$ are the resonant current through $L_{r1}$ and $L_{r2}$, respectively. The value of $i_p$ is the summation of the absolute value of $i_{L1}$ and $i_{L2}$. The inductor current $i_{L1}$, $i_{L2}$, i.e., the gate current of power MOSFET is sinusoidal and discontinuous, which reduces the additional conduction loss. The proposed RGD turns the MOSFETs on and off by using the resonant current injected into the input capacitance as shaded during $[t_1, t_2]$ and $[t_3, t_4]$. Moreover, the gate-to-source voltage $v_{gs\_Q1}$ and $v_{gs\_Q2}$ are complementary and sinusoidal during the switching transition.

![Diagram of key waveforms of the proposed RGD](image)

Fig. 6  Key waveforms of the proposed RGD

The operation principle of the proposed RGD includes four operating modes during one period as illustrated in Fig. 7 (a)-(d). $C_{g\_Q1}$ and $C_{g\_Q2}$ represent the input capacitance of power MOSFETs $Q_1$ and $Q_2$, respectively. Initially it is assumed that $Q_1$ is off and $Q_2$ is on before $t_0$ as shown in Fig. 7 (a).
1) Mode 1 \([t_0, t_1]\)

\(S_2\) and \(S_3\) conduct during this interval as illustrated in Fig. 7 (a). The voltage between \(A\) and \(B\), \(u_{AB}\) is clamped to \(-V_c\). As the ratio of the drive transformer is 1:1, the value of the gate-to-source voltage \(v_{gs\_Q_1}\) is initially charged at \(-V_c\). This negative gate drive voltage prevents the false trigger due to fast \(dv/dt\) problem in the FB converter. As the polarities of the secondary windings are opposite for the power MOSFETs \(Q_1\) and \(Q_2\), the gate-to-source voltage \(v_{gs\_Q_2}\) is initially charged at \(V_c\), and \(Q_2\) is on during this interval.

2) Mode 2 \([t_1, t_2]\)

At \(t_1\), since the resonant current starts from \(i_{Lr1}=i_{Lr2}=i_p=0\), \(S_3\) turns off with ZCS and \(S_4\) turns on with ZCS. The voltage \(u_{AB}=0\) and the voltage of the secondary windings is clamped to zero. With the initial electrostatic energy stored in the input capacitance, the resonance between the \(C_{g\_Q_1}\) and \(L_{r1}\), \(C_{g\_Q_2}\) and \(L_{r2}\) starts respectively as illustrated in Fig. 7 (b). It is observed that the drive current circulates among \(S_2\) and \(S_4\), \(L_{r1}\) and \(C_{g\_Q_1}\), \(L_{r2}\) and \(C_{g\_Q_2}\), and no current flows through the dc power supply \(V_c\). Therefore, the power supply provides no electric power to the gate drive circuit theoretically during the switching transition, which indicates that the gate drive loss is reduced significantly by the proposed RGD. During this interval, the power MOSFETs \(Q_1\) and \(Q_2\) operate in the complementary mode. At \(t_2\), \(v_{gs\_Q_1}\) reaches \(V_c\) and \(v_{gs\_Q_2}\) reaches \(-V_c\), \(Q_1\) turns on and \(Q_2\) turns off at the end of this interval.

3) Mode 3 \([t_2, t_3]\)

At \(t_2\), since the resonant transition ends when \(i_{Lr1}=i_{Lr2}=i_p=0\), \(S_2\) turns off with ZCS and \(S_1\) turns on with ZCS. As the voltage \(u_{AB}\) is clamped to \(V_c\), the voltage \(v_{gs\_Q_1}\) is actively clamped to \(V_c\), and \(v_{gs\_Q_2}\) is actively clamped to \(-V_c\) as illustrated in Fig. 7 (c). Therefore, \(v_{gs\_Q_1}=V_c\) and \(v_{gs\_Q_2}=-V_c\) remain unchanged during this interval. Therefore, this interval can be set to adjust the duty cycle.

4) Mode 4 \([t_3, t_4]\)

At \(t_3\), the resonant current starts from \(i_{Lr1}=i_{Lr2}=i_p=0\), \(S_1\) turns off with ZCS and \(S_2\) turns on with ZCS. This interval as illustrated in Fig. 7 (d) is similar to operation Mode 2 as shown in Fig. 7 (b). However, the direction of the resonant current \(i_{Lr1}, i_{Lr2}\) is opposite. At \(t_4\), \(v_{gs\_Q_1}\) reaches \(-V_c\) and \(v_{gs\_Q_2}\) reaches \(V_c\). So \(Q_1\) turns off and \(Q_2\) turns on at the end of this interval.
A. The Gate Drive Loss with the Proposed RGD

Fig. 8 shows the equivalent loss model of the proposed RGD, which includes the circuit elements producing the power consumption in the practical gate drive circuit. $R_{DS(on)}$ is the on-state resistance and $C_{oss}$ is the output capacitance in the drive MOSFETs; $S_1$-$S_4$. $R_g$ is the summation of the winding resistance in resonant inductor and transformer, and the gate-pattern resistance inside the power MOSFET. The damping resistance $R_d$ is connected in series with $S_1$ and $S_3$.

As the two power MOSFETs $Q_1$ and $Q_2$ are controlled in the complementary mode, the gate drive loss of $Q_1$ is chosen to analyze. The resonant inductor $L_{r1}$ and gate capacitance $C_{g,Q1}$ of $Q_1$ forms a series resonant circuit, in which the resonant angular frequency $\omega_R$ and resonant period $T_R$ are

$$\omega_R = \frac{1}{\sqrt{L_{r1}C_{g,Q1}}}$$  \hspace{1cm} (1)

$$T_R = \frac{2\pi}{\sqrt{L_{r1}C_{g,Q1}}}$$  \hspace{1cm} (2)
where $L_{r1}$ is the value of the resonant inductor and $C_{g\_Q1}$ is the value of the gate capacitance of $Q_1$.

Fig. 8 Loss analysis model of the proposed RGD

Fig. 8 shows the turn-on transition of the power MOSFET $Q_1$. With the operation principle of the proposed RGD presented in Section III, the gate current $i_{Lr1}$ flows through $S_2$ and $S_4$ with two $R_{DS(on)}$ and $R_{sg}$ during the turn-on transition, i.e. from $t_0$ to $t_2$. When $t_0=0$, the gate to source voltage $v_{gs\_Q1}$ is

$$v_{gs\_Q1} = -\frac{V_c}{2} \sqrt{4 + \omega_R^2 R^2 C_{g\_Q1}^2} \frac{e^{-(RC_{g\_Q1})/2}}{2} \cos \omega_R t$$

(3)

where $R$ is the total resistance and is given by $R=2R_{DS(on)}+R_{sg}$.

Due to the resistance energy loss of the resonant circuit, the amplitude of the gate-to-source voltage decreases and there is a voltage drop after each switching transition. The voltage drop is defined as $\Delta V$ as shown in Fig. 9. When $t_2=T_R/2$, $v_{gs\_Q1}$ reaches the maximum value during the turn-on transition. From (2)
and (3), with \( t_2 = T_d / 2 \), the value of \( \Delta V \) is

\[
\Delta V = V_c \left[ 1 - \frac{\sqrt{4 + \omega_c^2 R^2 C^2}}{2} e^{-\left(\frac{RC}{\omega_c^2} t_2\right)} \right]
\]  

(4)

At \( t_2 \), the drive MOSFET \( S_2 \) turns off and \( S_1 \) turns on as shown in Fig. 9. Then, the \( V_{gs_Q1} \) is clamped to \( V_c \) and the dc power supply provides an amount of electric energy, which is equal to \( C_{gs_Q1} V_c \Delta V \) for the turn-on procedure. In the same way, \( C_{gs_Q1} V_c \Delta V \) is also provided for the turn-off procedure. Therefore, the electric power to compensate for the voltage drop \( \Delta V \) is

\[
P_{e,RGD} = 2 f_{sw} C_{gs_Q1} V_c \Delta V
\]  

(5)

Although the total gate charge of \( S_1-S_4 \) is low, it may still cause some losses at high switching frequency. The switching frequency of these four MOSFETs is the same as the \( f_{sw} \) of the power MOSFETs. The total gate drive loss of \( S_1-S_4 \) is

\[
P_s = 4 Q_{gs_s} V_{gs_s} f_{sw}
\]  

(6)

where \( Q_{gs_s} \) is the total gate charge of drive MOSFETs, \( V_{gs_s} \) is the drive voltage of \( S_1-S_4 \).

In addition, the power loss \( P_r \) of the output capacitance \( C_{oss} \) in the drive MOSFETs \( S_1-S_4 \) is

\[
P_r = 4 C_{oss} V_c^2 f_{sw}
\]  

(7)

The transformer loss consists of the magnetic hysteresis loss, eddy-current loss and residual loss. The total transformer loss is

\[
P_i = \eta f_s^\alpha B_m^\beta V
\]  

(8)

where \( \eta \) is the loss coefficient, \( \alpha \) is the frequency index (>1), \( \beta \) is the magnetic induction index (>1), \( B_m \) is the magnetic induction, and \( V \) is the volume of the magnetic core.

From (5), (6), (7) and (8), the power consumption \( P_{d,RGD} \) for driving two MOSFETs in one bridge leg with the proposed RGD is

\[
P_{d,RGD} = 2P_{e,RGD} + P_s + P_r + P_i
\]  

(9)

B. The Gate Drive Loss Comparison between the Proposed RGD and Conventional VSD

For comparison, the conventional transformer coupled VSD in Fig. 2 is analyzed. The gate drive loss for one power MOSFET with the conventional VSD is calculated. Take account of the negative gate voltage,
the dc power supply has to provide an electric energy as large as \(2C_{Q_1}V_c^2\) to turn the power MOSFET on or off. This electric energy provided by the dc power supply is consumed in the gate resistor \(R_g\). Therefore, the power loss \(P_{c,VSD}\) in the gate resistor is

\[
P_{c,VSD} = 4f_{sw}C_{Q_1}V_c^2
\]

From (6), (7), (8) and (10), the power consumption for driving two MOSFETs in one bridge leg with the conventional transformer coupled VSD is

\[
P_d\text{ VSD} = 2P_{c,VSD} + P_s + P_t
\]

To demonstrate the gate drive loss reduction with the proposed RGD, the design parameters are given in TABLE I. The design parameters provided in this part agree with the experimental parameters.

### TABLE I: DESIGN PARAMETERS OF THE PROPOSED RGD

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency, (f_{sw})</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Gate Drive Voltage, (V_c)</td>
<td>15 V</td>
</tr>
<tr>
<td>Resonant Inductor, (L_{r1},L_{r2})</td>
<td>246 nH</td>
</tr>
<tr>
<td>Power MOSFET, (Q_1,Q_2)</td>
<td>IPP50R199CP</td>
</tr>
<tr>
<td>Total Gate Charge, (Q_g)</td>
<td>50 nC</td>
</tr>
<tr>
<td>Internal Gate Resistance, (R_g)</td>
<td>2.2 Ω</td>
</tr>
<tr>
<td>Drive MOSFETs, (S_1-S_4)</td>
<td>FDN335N</td>
</tr>
<tr>
<td>Total Gate Charge, (Q_{gs})</td>
<td>3.7 nC</td>
</tr>
<tr>
<td>On Resistance, (R_{DS(on)})</td>
<td>0.07 Ω</td>
</tr>
<tr>
<td>Output Capacitance, (C_{oss})</td>
<td>80 pF</td>
</tr>
</tbody>
</table>

Based upon the design parameters above, the calculated results are provided in the TABLE II. With the proposed RGD, the gate drive loss of two MOSFETs in one bridge leg is reduced from 3.2 W to 0.72 W (a reduction of 78%). As a result, the gate drive loss of four MOSFETs in a FB converters is reduced from 6.4 W to 1.44 W (a reduction of 78%), translating into an efficiency improvement of 0.5 percent in a 1-kW 500-kHz FB converter.

### TABLE II: GATE DRIVE LOSS CALCULATION COMPARISON BETWEEN THE PROPOSED RGD AND CONVENTIONAL VSD

<table>
<thead>
<tr>
<th></th>
<th>Conventional VSD</th>
<th>Proposed RGD</th>
<th>Loss Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Consumption for the Resistance (P_{c,VSD}, P_{c,RGD})</td>
<td>3 W ((P_{c,VSD}))</td>
<td>0.53 W ((P_{c,RGD}))</td>
<td>2.47 W (a reduction of 82%)</td>
</tr>
<tr>
<td>Gate Drive Loss of (S_1-S_4, P_t)</td>
<td>0.037 W</td>
<td>0.037 W</td>
<td>-</td>
</tr>
<tr>
<td>Power Loss of the Output Capacitance in (S_1-S_4, P_t)</td>
<td>0.036 W</td>
<td>0.036 W</td>
<td>-</td>
</tr>
<tr>
<td>Transformer Loss, (P_t)</td>
<td>0.12 W</td>
<td>0.12 W</td>
<td>-</td>
</tr>
<tr>
<td>Gate Drive Loss of Two MOSFETs in One Bridge Leg</td>
<td>3.2 W ((P_{d,VSD}))</td>
<td>0.72 W ((P_{d,RGD}))</td>
<td>2.48 W (a reduction of 78%)</td>
</tr>
<tr>
<td>Gate Drive Loss of Four MOSFETs in a FB Converter</td>
<td>6.4 W</td>
<td>1.44 W</td>
<td>4.96 W (a reduction of 78%)</td>
</tr>
</tbody>
</table>
C. The Switching Loss Comparison between the Proposed RGD and Conventional VSD

This section analyzes the potential switching loss reduction with the proposed RGD. In the ZVS FB converter, the turn-on loss is significantly reduced due to ZV turn on condition. However, there is still some turn-off loss normally. In the conventional VSD, the gate current decays significantly from its peak value due to the RC type charging and discharging as shown in Fig. 10. On the other hand, the gate current in the proposed RGD is sinusoidal as shown in Fig. 10.

![Comparison between the gate current for the conventional VSD and proposed RGD](image)

**Fig. 10** Comparison between the gate current for the conventional VSD and proposed RGD

For the conventional VSD, the turn-off switching loss, \( P_{\text{off, VSD}} \) is given approximated by (12). In (12), \( V_{ds} \) represents the voltage across the switch, \( I_{\text{off, pk}} \) is the peak current through the switch at turn off and \( t_{f, \text{VSD}} \) is the fall time given by (13). In (13), \( I_{\text{th, off}} \) is the gate current when the gate voltage is at the threshold and is given by (14). Also in (13), \( I_{\text{pl, off}} \) is the gate current when the gate voltage is at the plateau and is given by (15). \( t_{f, \text{VSD}} \), \( I_{\text{th, off}} \) and \( I_{\text{pl, off}} \) are clearly shown in Fig. 10. Other parameters include the power MOSFET total gate charge at the beginning of the plateau, \( Q_{\text{pl}} \), the total gate charge at the threshold, \( Q_{\text{th}} \), the gate to drain charge, \( Q_{\text{gd}} \), the MOSFET internal gate resistance, \( R_g \) and the external gate resistance in the drive circuit, \( R_{\text{ext}} \).

\[
P_{\text{off, VSD}} = \frac{1}{2} f_{s} V_{ds} I_{\text{off, pk}} t_{f, \text{VSD}}
\]  

(12)
\[ t_{f_{-}VSD} = \frac{Q_{pl} - Q_{th}}{2|I_{th_{-}off} + I_{pl_{-}off}|} + \frac{Q_{gd}}{|I_{pl_{-}off}|} \]  

(13)

\[ I_{th_{-}off} = \frac{V_{th}}{R_{ext} + R_{g}} \]  

(14)

\[ I_{pl_{-}off} = \frac{V_{pl}}{R_{ext} + R_{g}} \]  

(15)

On the other hand, for the proposed RGD with the sinusoidal gate current, the turn-off switching loss, \( P_{off_{-}RGD} \) is approximated by (16), where \( I_{g_{-}avg} \) is the average gate current during the turn-off transition, \( t_{f_{-}RGD} \).

In (17), \( I_{g_{-}pk} \) is the maximal gate current given by (18), \( t_{pl_{-}off} \) is the time when the gate voltage is at the plateau and is given by (19). Also in (17), \( t_{th_{-}off} \) is the time when the gate voltage is at the threshold and is given by (20). \( I_{g_{-}pk}, I_{pl_{-}off} \) and \( I_{th_{-}off} \) are clearly shown in Fig. 10. The shaded area between \( t_{pl_{-}off} \) and \( t_{th_{-}off} \) is the transition produces the switching loss in the proposed RGD. It is observed that the magnitude of the RGD current in this shaded area is greater than \( I_{pl_{-}off} \) and \( I_{th_{-}off} \), respectively. The result is that the turn-off time and the switching loss decrease. Other parameters noted include the input capacitance of the power MOSFET, \( C_{iss} \), the resonant inductor \( L_r \) and the gate drive voltage \( V_c \).

\[ P_{off_{-}RGD} = \frac{1}{2} f V_{ds} I_{off_{-}pk} \frac{Q_{pl} - Q_{th} + Q_{gd}}{|I_{g_{-}avg}|} \]  

(16)

\[ |I_{g_{-}avg}| = \int_{t_{th_{-}off}}^{t_{th_{-}off} - t_{pl_{-}off}} I_{g_{-}pk} \sin t dt = \frac{\cos t_{pl_{-}off} - \cos t_{th_{-}off}}{t_{th_{-}off} - t_{pl_{-}off}} I_{g_{-}pk} \]  

(17)

\[ I_{g_{-}pk} = \sqrt{\frac{C_{iss} V_c}{L_r}} \]  

(18)

\[ t_{pl_{-}off} = \arccos \frac{V_{pl}}{V_c} \]  

(19)

\[ t_{th_{-}off} = \arccos \frac{V_{th}}{V_c} \]  

(20)

The key design parameters of the proposed RGD are presented in TABLE I above. To demonstrate the potential switching loss reduction with the proposed RGD, the supplementary circuit parameters are listed in TABLE III.
TABLE III  CIRCUIT PARAMETERS FOR SWITCHING LOSS CALCULATION COMPARISON

<table>
<thead>
<tr>
<th>Converter Topology</th>
<th>ZVS FB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage across the MOSFET, $V_{ds}$</td>
<td>200 V</td>
</tr>
<tr>
<td>MOSFET Turn-off current, $I_{off(pk)}$</td>
<td>5 A</td>
</tr>
<tr>
<td>External Impedance, $R_{ext}$</td>
<td>2 Ω</td>
</tr>
<tr>
<td>Power MOSFET</td>
<td>IPP50R199CP</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>11 nC</td>
</tr>
<tr>
<td>$Q_{th}$</td>
<td>5 nC</td>
</tr>
<tr>
<td>$Q_{pl}$</td>
<td>7.5 nC</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>3 V</td>
</tr>
<tr>
<td>$V_{pl}$</td>
<td>5.2 V</td>
</tr>
<tr>
<td>$C_{iss}$</td>
<td>3300 pF</td>
</tr>
</tbody>
</table>

Base on (12) and (16), the switching loss of the conventional VSD and proposed RGD are calculated with the parameters in Table III respectively using the MATHCAD software. In TABLE IV, the switching loss of one MOSFET is reduced by 0.85 W (from 2.86 W to 2.01 W, a reduction of 30%). The total switching loss in the ZVS FB converter is reduced by 3.4 W (from 11.44 W to 8.04 W, a reduction of 30%). Therefore, the proposed RGD not only has a significant gate drive loss reduction, but also can achieve a switching loss reduction.

TABLE IV  SWITCHING LOSS CALCULATION COMPARISON BETWEEN THE PROPOSED RGD AND CONVENTIONAL VSD

<table>
<thead>
<tr>
<th></th>
<th>Switching Loss of One MOSFET in the ZVS FB Converter</th>
<th>Switching Loss of Four MOSFETs in the ZVS FB Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional VSD</td>
<td>2.86 W</td>
<td>11.44 W</td>
</tr>
<tr>
<td>Proposed RGD</td>
<td>2.01 W</td>
<td>8.04 W</td>
</tr>
<tr>
<td><strong>Switching Loss Reduction</strong></td>
<td><strong>0.85 W (a reduction of 30%)</strong></td>
<td><strong>3.4 W (a reduction of 30%)</strong></td>
</tr>
</tbody>
</table>

D. Optimal Design for the Proposed RGD

In the proposed RGD, the resonant inductance is the crucial component. The inductance value of $L_{r1}$ and $L_{r2}$ are assumed equal as $L_{r1} = L_{r2} = L_r$. When the switching frequency $f_{sw}$ is fixed, i.e. 500 kHz, the value of the resonant inductance $L_r$ remains to be determined. Therefore, three design rules need to be followed: 1) to ensure the resonant manner of the proposed RGD; 2) fast driving speed; 3) to minimize the overall loss of the gate drive loss and switching loss.

1) **Rule 1: To ensure the resonance of $L_r$-$C_{iss}$**

In the proposed RGD, to ensure that the total resistance $R$ in the drive circuit has no effect on the natural resonance between the resonant inductor $L_r$ and input capacitance $C_{iss}$, the characteristic impedance $R_{LC}$ of $L_r$ and $C_{iss}$ has to be large enough and should meet
\[ R_{LC} = \frac{L_r}{\sqrt{C_{iss}}} = (2 \sim 3) \times R \] (21)

where \( R \) is the summation of the winding resistance in resonant inductor and transformer, the gate-pattern resistance inside the power MOSFET and the on-resistance of the drive MOSFETs.

From (21), the value of the resonant inductor \( L_r \) can be calculated as

\[ L_r = [(2 \sim 3) \times R]^2 \times C_{iss} \] (22)

From (22), based on the circuit parameters from TABLE I, the value of the resonant inductor \( L_r \) can be solved to be larger than 240 nH (\( L_r \geq 240 \text{ nH} \)).

2) **Rule 2: Fast driving speed**

The value of \( L_r \) affects the rising time \( t_r \) and falling time \( t_f \) of driving a power MOSFET, i.e. the switching speed. In the proposed RGD, as the characteristic impedance \( R_{LC} \) is much larger than the total resistance \( R \) in the resonant circuit, the gate drive voltage of power MOSFET \( Q_1 \) or \( Q_2 \) can be regarded as sinusoidal during the turn on transition. As shown in Fig. 11, the rising time \( t_r \) defined as the interval for \( v_{gs} \) to rise from zero to \( V_c \) is

\[ t_r = \frac{1}{2} \pi \sqrt{\frac{L_r}{C_{iss}}} \] (23)

Similarly, the falling time \( t_f \) defined as the interval for \( V_{gs} \) to fall from \( V_c \) to zero is

\[ t_f = \frac{1}{2} \pi \sqrt{\frac{L_r}{C_{iss}}} \] (24)

![Fig. 11 t_r and t_f during the switching period](image)

From (23) and (24), it is noted that the larger \( L_r \) is, the slower the power MOSFET can be driven. Considering ZVS operation of one bridge leg, less than 5% of the switching period is usually allowed as (25)
\[ t_d = t_r + t_f = \pi \sqrt{\frac{L_r}{C_{\text{iss}}}} \leq \frac{5\%}{f_s} \]  \tag{25}

where \( t_d \) is the total driving time of the power MOSFET.

From (25), the maximal value of \( L_r \) is solved

\[ L_r \leq \frac{\left(\frac{5\%}{\pi f_s}\right)^2}{C_{\text{iss}}} \]  \tag{26}

Based upon the given design parameters in TABLE I, the value of \( L_r \) can be calculated to be less than 300 nH (\( L_r \leq 300 \text{ nH} \)).

In summary, from the design Rule 1 and Rule 2, the accepted design range for \( L_r \) is from 240 nH to 300 nH as illustrated in Fig. 12.

![Fig. 12 The design requirement of Rule 1 and Rule 2](image)

3) **Rule 3: To minimize the overall loss of the gate drive loss and switching loss**

From (9), the power consumption \( P_{d\_RGD} \) is the gate drive loss for driving two MOSFETs in one bridge leg. From (16), the power consumption \( P_{\text{off\_RGD}} \) is the turn-off switching loss, i.e. the switching loss for one MOSFET. Then, the switching loss \( P_{\text{sw\_RGD}} \) for two power MOSFETs in one bridge leg is

\[ P_{\text{sw\_RGD}} = 2P_{\text{off\_RGD}} \]  \tag{23}

Then, the overall loss of the gate drive loss and switching loss in one bridge leg, \( P_{\text{sum}} \) is

\[ P_{\text{sum}} = P_{d\_RGD} + P_{\text{sw\_RGD}} \]  \tag{24}

From (9), (16), (23) and (24), \( P_{d\_RGD}, P_{\text{sw\_RGD}} \) and \( P_{\text{sum}} \) as function of the resonant inductance \( L_r \) are
illustrated in Fig. 13. From Fig. 13, it is observed that with the increase of the resonant inductance $L_r$, the gate drive loss $P_{d_{RGD}}$ is reduced. The reduction slew rate of the gate drive loss tends to be slow when $L_r$ becomes large. With the increase of $L_r$, the switching loss $P_{sw_{RGD}}$ increase. At the same time, the overall loss $P_{sum}$ of the gate drive loss and switching loss also increase since the switching loss is the dominate element compared to the gate drive loss.

![Fig. 13 $P_{d_{RGD}}, P_{sw_{RGD}}$ and $P_{sum}$ as functions of the resonant inductance $L_r$](image)

Fig. 13  $P_{d_{RGD}}, P_{sw_{RGD}}$ and $P_{sum}$ as functions of the resonant inductance $L_r$

As a conclusion, in order to minimize the overall loss of the gate drive loss and the switching loss, the resonant inductance $L_r$ should to be chosen as small as possible in the accepted range. Therefore, the value of $L_r$ is about 240 nH for the optimum design in the proposed RGD with the desired specifications.

### E. Dead Time Control in the Proposed RGD

Since the proposed RGD is used to drive the HB leg, the dead time should be inserted to avoid the short-through. The waveforms of the gate drive voltage of $Q_1$ and $Q_2$ are shown in Fig. 6. It is observed that the waveforms of gate drive voltage of $Q_1$ and $Q_2$ are complementary. When $v_{gs_{Q1}}$ changes from the positive maximum value to the negative maximum value, $v_{gs_{Q2}}$ changes from the negative maximum value to the positive maximum value simultaneously. As a result, there is no voltage overlap between two drive voltage signals, which prevents the short-through during the dead time. Considering the tolerance of the input capacitance of $Q_1$ and $Q_2$ in practical applications, the value of two resonant inductors in each RGD can be adjusted to guarantee enough dead time between two complementary signals. Moreover, since different resonant inductor values lead to different resonant periods and this can be used to obtain desired dead time according to the applications.
V. THE COMPARISON BETWEEN THE PROPOSED RGD AND PREVIOUS GATE DRIVE CIRCUITS

A. Operation Comparison between the Proposed RGD and Conventional Transformer Coupled VSD

The transformer coupled VSD is shown in Fig. 2. This VSD can be used with either coreless or core-based transformer. The coreless transformer in [30] simplifies the VSD and performs virtually as well as its core-based counterpart, however it is still a VSD based driver and has no capability to recovery high frequency gate drive loss. The proposed isolated RGD is shown in Fig. 5 above. The two gate drive circuits are both able to drive two power MOSFETs. Considering the leakage inductance of the transformer, the simplified equivalent circuit of the transformer coupled gate driver during the turn on transition is shown in Fig. 14 (a). For comparison, the simplified equivalent circuit of the proposed RGD during the turn on transition is shown in Fig. 14 (b).

![Fig. 14: The simplified equivalent circuits during the turn-on transition](image)

For comparison, in the transformer coupled VSD as shown in Fig. 14 (a), $C_{iss}$ represents the input capacitance of the power MOSFET. The inductance $L_k$ consists of the leakage inductance and stray inductance, which is as a disadvantageous element. $R_g$ is the gate mesh resistance of the power MOSFET and $R_{ext}$ is the external damping resistance. Due to the existence of the inductance, the gate-to-source voltage $v_{gs}$ is oscillating during the charging and discharging intervals. Therefore, the external resistance $R_{ext}$ has to be inserted in the gate drive circuit to damp the oscillation and make the $R-L-C$ second-order system under the overdamping condition. But the problem is that the external resistance slows down the driving speed and increases the switching loss.

In the proposed RGD as shown in Fig. 14 (b), the resistance is only the gate mesh resistance of the power MOSFET. The leakage inductance of the drive transformer and stray inductance no longer exist as the disadvantageous elements. The proposed RGD utilizes the $L-C$ resonance to recover the charge energy.
of the input capacitance. An additional resonant inductance $L_r$ may also be applied to adjust the value of the total inductance for the optimum design.

The operation principles of the transformer coupled VSD and the proposed RGD are quite different. The key point of the gate drive energy recovery in the proposed RGD is the different control strategy from the transformer coupled VSD. Unlike the VSD, the proposed RGD can provide an additional interval in the switching transition, when the primary-side voltage $u_{ds}$ of the drive transformer is zero as shaded area in Fig. 6. During this interval, the proposed RGD utilizes the energy stored in the gate capacitance instead of the drive voltage supply to switch the polarities of the gate voltage through the energy exchange in the resonance manner. However, the VSD operates in the overdamping mode as a $R-L-C$ second-order system during the charging and discharging period. The energy provided by the dc power supply $V_c$ is entirely dissipated in the damping resistance, which increases the gate drive loss. Based on the analysis above, the difference between the conventional VSD and the proposed RGD is summarized in TABLE V.

Particularly, for the coreless driver in [30], it is still a conventional voltage source driver and the leakage inductance in the coreless PCB transformer has negative effective on the driver performance and should be minimized. As comparison, the proposed RGD can take advantage of the leakage inductance to build the resonance with the gate capacitance of the power MOSFET so that the gate energy recovery and turn off loss reduction can be achieved.

| TABLE V THE COMPARISON BETWEEN THE CONVENTIONAL TRANSFORMER COUPLED VSD AND PROPOSED RGD |
|---------------------------------------------------------------|---------------------------------------------------------------|
| Control Strategy in the Switching Transition                 | The Conventional Transformer Coupled VSD                     |
|                                                              | Utilize the DC power supply to change the gate-to-source voltage |
|                                                              | Provide an additional interval for the $L-C$ resonance to recover gate energy |
| Energy Stored in $C_{iss}$                                   | Dissipated in the damping resistance totally                  |
|                                                              | Recovered by utilizing the $L-C$ resonance, reduce gate drive loss significantly |
| Leakage Inductance of the Transformer, $L_k$                 | A disadvantageous element, make the drive voltage to be oscillating |
|                                                              | Be utilized to recover the gate drive energy                   |
| External Damping Resistance, $R_{ext}$                       | Should be inserted to damp the oscillation, slow down the driving speed, increase switching loss |
|                                                              | Not needed                                                     |

B. The Comparison between the Proposed Isolated RGD and the RGD in [24]

As analysed in Session II, the RGD in [24] is one of the candidates for the FB converter. The advantages of this RGD include: 1) it reduced the power consumption by a factor of ten, compared with a conventional VSD; 2) the negative drive voltage provided by this RGD can prevent the false trigger.
However, the RGD in [24] needs much more devices than the proposed isolated RGD. The number of drive switches and independent dc power supplies required to drive a FB converter are compared as shown in TABLE VI. Essentially, the RGD in [24] needs sixteen drive switches and four independent dc power supplies for a FB converter. The proposed isolated RGD needs eight drive switches and one independent dc power supply. It is observed that the proposed isolated RGD needs much less drive switches and power supplies, which can minimize the cost and increase the reliability.

<table>
<thead>
<tr>
<th></th>
<th>Number of Drive Switches</th>
<th>Number of Independent DC Power Supplies</th>
</tr>
</thead>
<tbody>
<tr>
<td>RGD in [24]</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>Proposed RGD</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Reduction</td>
<td>50 %</td>
<td>75 %</td>
</tr>
</tbody>
</table>

C. Comparison between the proposed RGD and conventional VSD with different switching frequencies and gate charge

The comparison between the proposed RGD and conventional VSD with different switching frequencies and different gate charge is illustrated as follows. The gate drive loss calculation of the proposed RGD and conventional VSD in this section is based on the equations presented in section IV.

Fig. 15 shows the relationship between the switching frequency \( f_{sw} \) and the gate drive loss for one bridge leg \( P_{d,leg} \). The gate drive loss for one bridge leg with the proposed RGD is given in (9) and the gate drive loss for one bridge leg with the conventional VSD is given in (11). As the frequency increases, the loss in both gate drivers becomes large proportionally. However, the gate drive loss can be reduced significantly with the proposed RGD. Furthermore, when the switching frequency increases higher, more loss can be saved by the proposed RGD as shown in Fig. 15.

![Fig. 15 The relationship between the switching frequency and gate drive loss](image-url)
The NMOSFET IPP50R199CP ($V_{DS}=550$ V, $I_D=17$ A, $Q_g=50$ nC) from Infineon is chosen as the power MOSFET in the experimental prototype in this paper. It is noted that not only this power MOSFET, other power MOSFETs can be driven by the proposed RGD in different applications. In high current applications, to reduce the on-state resistance of the power MOSFET, the super junction structure is introduced in MOSFETs, which increase the gate charge $Q_g$ and the input capacitance $C_{iss}$ of the power MOSFET. Fig. 16 shows the gate drive loss $P_{d,\text{leg}}$ for one bridge leg as a function of the gate charge $Q_g$. The gate drive loss for one bridge leg with the proposed RGD is given in (9) and the gate drive loss for one bridge leg with the conventional VSD is given in (11). It is observed that as the gate charge increases, the gate drive loss in both gate drivers is increasing correspondingly. In addition, under larger gate charge situations, the more gate drive loss can be reduced by the proposed RGD. For example, the gate charge $Q_g$ of the CoolMOS™ SPW52N50C3 ($V_{DS}=560$ V, $I_D=52$ A) from Infineon is 290 nC. From (9) and (11), about 11.4 W can be reduced by the proposed RGD as shown in Fig. 16. Therefore, with the proposed RGD, a more significant gate drive loss reduction can be achieved in larger gate charge situations.

![Diagram](image)

**Fig. 16** The relationship between the gate charge and gate drive loss

### D. Benefits of the Proposed RGD

With the above comparison, the advantages of the proposed isolated RGD are highlighted as follows:

1) **Significant reduction of gate drive loss**

Compared to the conventional gate driver, the energy stored in the input capacitance can be recovered in the proposed RGD. The resonance between the resonant inductor and input capacitance makes the energy...
to return to the input capacitance and reverses the polarity of the input capacitance.

2) **High reliability of the turn-off status**

The RGD is able to provide a negative gate voltage to the MOSFET and improves the reliability due to fast \( dv/dt \) problem in high power and high voltage applications.

3) **Capability to provide two isolated complementary drive signals**

The proposed RGD has the ability to drive two MOSFETs in a bridge-leg and makes the power segment and control segment to be isolated, which leads to the simplicity and low cost.

### E. Applications Extension

The proposed RGD is able to provide two isolated complementary drive signals for a pair of power MOSFETs. Therefore, it is not only suitable for the traditional ZVS FB converters, but also can be applied to other ZVZCS converters at a higher power level. Two structures of ZVZCS converters presented in [31] and [32] operate in a higher power level and have a good efficiency. Fig. 17 (a) shows the proposed RGD applied to the ZVZCS converter in [31], in which each pair of power MOSFETs \( Q_1 \) and \( Q_2 \), \( Q_3 \) and \( Q_4 \), \( Q_5 \) and \( Q_6 \) requires two complementary drive signals. Similarly, Fig. 17 (b) shows the proposed RGD applied to the converter in [32]. The proposed RGD can be applied to these ZVZCS converters to reduce the gate driver loss and turn off loss at high switching frequency.

![Fig. 17 The ZVZCS converters in [31] and [32] with the proposed RGD](image-url)
In addition, there are some applications, in which the gate drive loss deserves a lot more attention. For example, the large gate charge $Q_g$ of the synch FETs in Voltage Regulators (VRs) leads to excessive gate drive loss at the high switching frequency [33]. The gate drive loss in the very high frequency (VHF) dc/dc converters is a large proportion in the total loss [34]-[36] and therefore, the RGD solution needs to be applied.

VI. SIMULATION RESULTS AND DISCUSSION

A ZVS FB converter spice simulation model with the proposed RGD has been developed. The specifications of the proposed RGD are as follows: the switching frequency $f_{sw}$=500 kHz; the gate drive voltage $V_c$=15 V; the resonant inductor $L_r$=246 nH; the total gate charge $Q_g$=50 nC; the equivalent input capacitance $C_{iss}$=3.3 nF and the internal gate resistance $R_g$=2.2 Ω.

Fig. 18 shows the driving signals of $S_1$-$S_4$ and the primary-side voltage $v_{AB}$. It is observed that the waveforms of $S_1$ and $S_2$ are complementary, as well as $S_3$ and $S_4$. When $S_1$ and $S_4$ turn on, the value of $v_{AB}$ is negative maximum; when $S_2$ and $S_3$ turn on, the value of $v_{AB}$ is positive maximum; when $S_2$ and $S_4$ turn on, $v_{AB}$=0 and this is the switching transition of the proposed RGD, which agrees with the key waveforms shown in Fig. 6.

![Driving signals of $S_1$-$S_4$ and $v_{AB}$](image)

The waveforms of the gate drive voltage and current are shown in Fig. 19. It is observed that in the switching transition, the waveforms of the resonant gate current and voltage are sinusoidal. Furthermore, when the inductor current changes to the highest value, the gate drive voltage becomes zero. The waveforms of $Q_1$ and $Q_2$ are complementary, which makes it possible to drive a HB leg. Meanwhile, there is no voltage overlap between two drive voltage signals, which prevents the short-through during the dead time.
Fig. 19 The waveforms of gate drive voltage and current

VII. EXPERIMENTAL RESULTS AND DISCUSSION

A 200-VDC input, 48-V/20-A output and 500-kHz phase-shift ZVS FB converter with the proposed RGD was built to verify the advantage. The schematic of the FB converter with the proposed RGD is shown in Fig. 20. The components used are as follows: IPP50R199CP is used as the power MOSFET $Q_1$-$Q_4$; the Schottky diode DSSK60-02A is used as the rectifier $D_{R1}$ and $D_{R2}$; the output inductance $L_f$ is 6 uH and the output capacitance $C_f$ is 63 V, 3000 uF. The FDN335N is used as the drive switch $S_1$-$S_8$ and the gate drive voltage $V_c = 15$ V. The magnetic core of the drive transformer $T_{r1}$ and $T_{r2}$ is EE 13. The turn ratio of $T_{r1}$ and $T_{r2}$ is 1:1. The magnetic inductance is 66.5 uH and leakage inductance is 246 nH, which are measured by the HEWLETT PACKARD 4284A precision LCR meter. Because the value of the leakage inductance fits the optimum design range, they can be used as the resonant inductance $L_{r1}$ and $L_{r2}$ in this case. The photo of the prototype is shown in Fig. 21.

Fig. 20 Complete schematic of the FB converter with the proposed RGD
Fig. 21 Photograph of the prototype

Fig. 22 illustrates the voltage of primary-side $v_p$ and the rectifier voltage $v_{rect}$ of the power transformer in the FB converter. It is observed that the primary voltage $v_p$ is a modulated pulse waveform since the phase-shift control is applied to the ZVS FB converter through the proposed RGD. The corresponding waveform of the secondary side $v_{rect}$ is obtained through the full-wave rectifier.

Fig. 22 The waveforms of $v_p$ and $v_{rect}$

Fig. 23 illustrates the drain-source voltage $v_{DS1}$ and the gate-source voltage $v_{GS1}$ of the power MOSFET $Q_1$ in the FB converter. Fig. 23 (a) shows that the FB converter realizes ZVS for the leading leg under 1/2 load. As the output capacitance of the main power MOSFET is discharged by the energy of the output inductance, the drain-to-source voltage $v_{DS}$ reaches zero, and then the gate drive voltage is applied to turn on the MOSFET with ZVS. Similarly, Fig. 23 (b) illustrates $v_{DS3}$ and $v_{GS3}$ of the power MOSFET $Q_3$ in the FB converter. This waveforms show that the FB converter realizes ZVS for the lagging leg under 2/3 load. The proposed RGD is compatible with ZVS technique for the FB converter, and the switching loss and the gate
drive loss can be both reduced.

Fig. 23 The waveforms of ZVS

Fig. 24 shows the resonant inductor current $i_{L_1}$ and the gate-to-source voltage $v_{gs_{Q1}}$. The waveforms of $i_{L_1}$ and $v_{gs_{Q1}}$ are sinusoidal during the switching transition, which indicates the resonance between the resonant inductor and the input capacitance of the main power MOSFET. It is observed that when $Q_1$ is off, the gate drive voltage $v_{gs_{Q1}}$ is -15 V, which improves the reliability due to fast $dv/dt$ problem in the FB converters.

Fig. 25 shows the resonant inductor current $i_{L_1}$, $i_{L_2}$ and the gate drive voltage $v_{gs_{Q1}}$, $v_{gs_{Q2}}$, which agrees with the theoretic waveforms in Fig. 6. It is observed that the gate drive voltage $v_{gs_{Q1}}$ and $v_{gs_{Q2}}$ are complementary, the directions of the resonant inductor current $i_{L_1}$ and $i_{L_2}$ are also opposite. This experimental waveform indicates that the proposed RGD has the ability to drive two power MOSFETs in
one bridge leg, leading to the low complexity and cost in the FB converters.

![Fig. 24 Gate drive voltage and resonant inductor current](image)

Fig. 24 Gate drive voltage and resonant inductor current

![Fig. 25 Two complementary drive voltage and resonant inductor current](image)

Fig. 25 Two complementary drive voltage and resonant inductor current

Fig. 26 (a) illustrates the relationship between \( v_{gs,Q1}, \) \( i_{Lr} \) and the voltage between \( A \) and \( B, v_{AB} \) during the turn on interval. It is observed that the resonance only happens during the stage of \( v_{AB}=0 \). This interval, i.e. \( v_{AB}=0 \), is the key difference between the conventional VSDs from the control strategy. During this interval, the proposed RGD utilizes the L-C resonance to recover the gate drive energy stored in the input capacitance of the power MOSFET. Therefore, the gate drive loss can be reduced significantly compared to the conventional VSDs. For the turn off interval, the detailed waveforms are provided in Fig. 26 (b), and they are similar to the turn on interval.
Fig. 26 Resonant switching transition: $v_{gs, Q1}$, $i_{Lr}$ and $v_{AB}$

Fig. 27 shows the waveforms of the gate drive voltage of $Q_1$ and $Q_2$. It is observed that the waveforms of gate drive voltage of $Q_1$ and $Q_2$ are complementary and there is no voltage overlap between two drive voltage signals. Therefore, the short-through problem can be prevented in the FB converters.
Fig. 27 Gate drive voltage of $Q_1$ and $Q_2$

Fig. 28 shows the measured efficiency comparison between the proposed RGD and conventional transformer coupled VSD. It is observed that at 4 A, the efficiency is improved from 84.7% to 86.7% (an improvement of 2.0%). At 12 A, the efficiency is improved from 91.4% to 92.2% (an improvement of 0.8%). It should be also noted that because of the low gate drive loss, the proposed RGD improves the efficiency effectively in full load range over the conventional transformer coupled VSD.

VIII. CONCLUSION

An isolated RGD for two MOSFETs in one bridge-leg is proposed in this paper. The proposed RGD can provide two complementary drive signals to drive two MOSFETs, which can be used to drive the HB leg in FB converters. The proposed RGD consumes no electric power theoretically. Moreover, with the negative drive voltage capability, the proposed RGD ensures high reliability in the FB converters over the
previously proposed RGDs. The loss analysis of the proposed isolated RGD and comparison between the conventional gate driver are provided. The optimal design procedure is presented in detail. A 200-V input, 48-V output and 500-kHz phase-shift ZVS FB converter was built to verify the advantages of the proposed isolated RGD. Compared with the conventional gate driver, the proposed isolated RGD improves the efficiency from 84.7% to 86.7% (an improvement of 2.0%) at 4 A, and at 12 A, from 91.4% to 92.2% (an improvement of 0.8%).

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2009.

