A Resonant Gate Drive Circuit

with Reduced MOSFET Switching and Gate Losses

Presented and Authored By:

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Co-Authors:

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1. **Introduction**
   1. *Why you should use resonant gate drive*
   2. *Drawbacks of existing techniques*

2. **Proposed Resonant Gate Driver and Operation**

3. **Logic Implementation**

4. **Design Procedure**

5. **Loss Analysis**

6. **Simulation and Experimental Results**

7. **Conclusions**
1. Introduction

- **Application**: low voltage high current DC-DC power supplies

- **Trend to increase switching frequency** for improvements in:
  + power density
  + dynamic performance

- **Drawbacks of increased switching frequency**:
  - gate loss
  - switching loss
Conventional MOSFET Driver

MOSFET Driver

Power MOSFET
parasitics in blue

Gate Loss

\[ P_{\text{gate}} = Q_g V_{GS} f_s \]

\[ P_{\text{switch}} = \frac{1}{2} (t_{\text{rise}} + t_{\text{fall}}) V_{DS} I_{DS} f_s \]

\[ P_{\text{out}} = \frac{1}{2} C_{DS} V_{DS}^2 f_s \]

MOSFET, or BJT switches

Hard Switching Waveforms

Switching Loss

\[
\begin{align*}
P_{\text{switch}} &= \frac{1}{2} (t_{\text{rise}} + t_{\text{fall}}) V_{DS} I_{DS} f_s \\
P_{\text{out}} &= \frac{1}{2} C_{DS} V_{DS}^2 f_s
\end{align*}
\]
Techniques for Improvement

Switching Loss Savings

Soft-Switching and Resonant Techniques

+ Well established and generally, have good performance
- Additional components
- Additional conduction loss
- Don’t reduce turn-off loss

Another Solution: Decrease switching time!

• Recall, switching loss proportional to rise time and fall time
Techniques for Improvement

Gate Loss Savings

Resonant Gate Drive Techniques

+ Many good (~15) circuits proposed since early 1990s, but generally unused

• Existing methods emphasize gate energy savings, but ignore potential switching loss savings

CURRENT SOURCE DRIVERS CAN REDUCE TURN-ON AND TURN-OFF LOSS!
Conventional vs. Resonant Drive
Switching Loss Savings

Gate Current
- Voltage source
- RC-type charging
- limits speed

Gate Voltage
- Constant current source
- type charging
- improves speed!
Actual driver loss can be much higher than CV$^2$ loss… e.g. varies by driver, but typically 15-50%

$$P_{gate} = Q_g V_{GS} f_S$$

1. Additional Switching Loss
2. Additional Gate Loss
Actual Total Loss

<table>
<thead>
<tr>
<th>Loss/RMS Loss</th>
<th>CV2 RMS Loss</th>
<th>Control Switch Hard Switching Loss</th>
<th>Control Switch Gate Loss</th>
<th>Total Gate Circuit Loss</th>
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<tbody>
<tr>
<td></td>
<td>1.00</td>
<td>0.31</td>
<td>0.23</td>
<td>1.54</td>
</tr>
</tbody>
</table>
Existing techniques suffer from at least one of five problems:

2. Peak current dependent on duty cycle [2]
3. Large inductance [2], bulky transformer, or coupled inductor [3]-[7]

4. Slow turn-on and/or turn-off [3]-[9]

5. Gate not actively clamped high and/or low, so false triggering ($Cdv/dt$) can result [3]-[7], [9]
1. Introduction

2. Proposed Resonant Gate Driver and Operation
   - Circuit and waveforms

3. Logic Implementation

4. Design Procedure

5. Loss Analysis

6. Simulation and Experimental Results

7. Conclusions
Proposed Driver Evolution

- $v_{GS}$
  - Actively Clamped to $V_{cc}$
  - Constant Current for Quick Turn-On

- $I_{GS}$
  - Desired
  - Constant Current for Quick Turn-Off

- $I_{LR}$
  - Achieved
  - Circulating Current
  - Pre-Charge Turn-On Current Level

- $I_{LR}$
  - Proposed
  - No Circulating Current
  - Pre-Charge Turn-Off Current Level

Diagram:
- $V_{CC}$
- $Q_2$
- $L_R$
- $Q_1$
- $Q_4$
- $Q_3$
- $Q$
Turn-On Sequence

Switches Can Also Be Used Instead of Diodes
Turn-On Sequence

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Switches Can Also Be Used Instead of Diodes
Turn-Off Sequence

- $V_{CC}$
- $L_R$
- $Q_1$
- $Q_2$
- $Q_3$
- $Q_4$

Timing intervals:
- $t_4$ to $t_5$

Waveforms:
- $I_{LR}$
- $v_{GS}$
- $I_{VCC}$

Event markers:
- Energy from the Line
- Energy Returned to the Line

Time intervals:
- $t_0$ to $t_1$
- $t_2$ to $t_3$
- $t_4$ to $t_5$
- $t_6$ to $t_7$
- $t_7$ to $t_0$
Turn-Off Sequence

Diagram showing the turn-off sequence with key events labeled as follows:

- $V_{CC}$
- $Q_1$
- $Q_2$
- $Q_3$
- $Q_4$
- $L_R$
- $t_5-t_6$

Time intervals and waveforms are indicated with:

- $I_{LR}$
- $v_{GS}$
- $I_{VCC}$

Energy flow is marked as:

- Energy from the Line
- Energy Returned to the Line

The diagram illustrates the sequence of events during the turn-off process.
Turn-Off Sequence
Turn-Off Sequence

\[ V_{CC} \]

\[ Q_1 \]

\[ L_R \]

\[ Q_2 \]

\[ Q_3 \]

\[ Q_4 \]

\[ t_{7-t_0} \]

\[ I_{LR} \]

\[ v_{GS} \]

\[ I_{VCC} \]

Energy from the Line

Energy Returned to the Line

\( t_0 \) \( t_1 \) \( t_2 \) \( t_3 \) \( t_4 \) \( t_5 \) \( t_6 \) \( t_7 \) \( t_0 \)
1. Introduction
2. Proposed Resonant Gate Driver and Operation
3. Logic Implementation
   • Circuit and waveforms
4. Design Procedure
5. Loss Analysis
6. Simulation and Experimental Results
7. Conclusions
Implementation can be discrete with Fairchild Ultra High Speed (UHS) gates, or using a CPLD, or ultimately integrated into the driver IC.
1. Introduction

2. Proposed Resonant Gate Driver and Operation

3. Logic Implementation

4. Design Procedure
   1. Design steps

5. Loss Analysis

6. Simulation and Experimental Results

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Needed For Implementation:
1) Resonant Inductance, $L_R$
2) Delay Time, $TD_1$
3) Delay Time, $TD_2$
Design Procedure

Assumptions:
1) \( R_{ds} = R_g = 0 \)
2) Piecewise linear approximation

3 Equations:

\[ V_{cc} = L_R \frac{i_{LR}(t_1)}{T_{D1}} \quad (a) \]

\[ \Delta i_{LR} = \frac{V_{cc} \cdot t_{on}}{2 \cdot L_R} \quad (b) \]

\[ i_{LR}(t_1) = \frac{Q_g}{t_{on}} - \frac{\Delta i_{LR}}{2} \quad (c) \]
Design Procedure

1. Choose switches; 20V, 2A pk, low Qg & Rds < 250mΩ e.g. Fairchild NDS351AN and FDN352AP

2. Set ton; on time

3. Set TD1; turn-on pre-charge time

4. Calculate $\Delta i_{LR}$; solving (a)-(c)

5. Calculate $L_R$; using (b)

3 Unknowns in (a)-(c):

$\Delta i_{LR}$, $L_R$, $i_{LR}(t_1)$

(a) $V_{cc} = L_R \frac{i_{LR}(t_1)}{TD1}$

(b) $\Delta i_{LR} = \frac{V_{cc} t_{on}}{2 L_R}$

(c) $i_{LR}(t_1) = \frac{Q_g}{t_{on}} - \frac{\Delta i_{LR}}{2}$
Presentation Overview

1. Introduction
2. Proposed Resonant Gate Driver and Operation
3. Logic Implementation
4. Design Procedure
5. Loss Analysis
   1. Equations covered in paper
   2. Loss components
   3. Analysis results
6. Simulation and Experimental Results
7. Conclusions
Loss Analysis

Straightforward Calculations:

1. **Conduction loss in Q1-Q4, and Rg during 3 turn-on intervals and 3-turn-off intervals**
2. **Gate loss in Q1-Q4**
3. **CV^2 output loss in Q2 and Q4 at turn-on (small)**
4. **Turn-off loss in Q2 and Q4 (small)**
5. **Inductor core loss and logic loss (negligible)**
Loss Breakdown

Theoretical gate energy recovery at 1MHz
(parameters given in paper using design example)
Impact of $R_g$

Theoretical gate energy recovery at 1MHz

(parameters given in paper)
Recovery vs. Speed Tradeoff

Theoretical gate energy recovery at 1MHz
(parameters given in paper)
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SIMETRIX Simulation Results:
1MHz, IRF6618, $L_R=800\text{nH}$, $TD_1=40\text{ns}$, $ton=100\text{ns}$

Line Current
Q1
Q3
Q2
Q4
Inductor Current
MOSFET Vgs

Energy Recovered
Boost Experimental Results:
1MHz, IRF6618 (x2), 10TQ035 Diode, Vin=5V, Vo=10V

<table>
<thead>
<tr>
<th>Load Current [A]</th>
<th>Efficiency [%]</th>
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<tbody>
<tr>
<td>1</td>
<td>76.0</td>
</tr>
<tr>
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<td>8.5</td>
<td>83.5</td>
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<tr>
<td>9</td>
<td>84.0</td>
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</tbody>
</table>

- **Vcc=5V**
- **4% improvement**

- **L_R=105nH**
- **TD1=20ns**
- **Ton=55ns**
Boost Experimental Results:
1MHz, IRF6618 (x2), 10TQ035, Vin=5V, Vo=10V

Vcc=12V

6.5% improvement

L_R=285nH
TD1=25ns
Ton=100ns

Efficiency [%]

Load Current [A]
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Conclusions

New Resonant Driver Proposed:

- **Gate Energy Recovery**
- **Switching Loss Reduction**
- **Specific Advantages:**
  - Very small inductor (e.g. 100nH @ 1MHz)
  - Peak current independent of duty cycle
  - Low circulating current (discontinuous $I_{LR}$)
  - Quick turn on & off due to inductor pre-charge current during TD1
  - No $CdV/dt$ false triggering (low impedance)

- **4% efficiency improvement at 5V drive and 6.5% at 12V drive**
Thank You For Your Time

Other Resonant Gate Drive Material at:

www.queenspowergroup.com