A New Resonant Gate Drive Circuit with Efficient Energy Recovery and Low Conduction Loss

Wilson Eberle, P.C. Sen and Yan-Fei Liu
Queen’s Power Group, www.queenspowergroup.com
Department of Electrical and Computer Engineering, Queen’s University, Kingston, Ontario, Canada, K7L 3N6
wilson.eberle@wilson.eberle.com, senp@post.queensu.ca and yanfei.liu@ece.queensu.ca

Abstract - In this paper, a new resonant gate drive circuit is proposed. The proposed circuit consists of four control switches and a small resonant inductance. The current through the resonant inductance is discontinuous in order to minimize circulating current conduction loss present in other methods. The proposed circuit also achieves quick turn-on and turn-off transition times to reduce switching loss and conduction loss in power MOSFETs. An analysis, design procedure and simulation results are presented for the proposed circuit.

I. INTRODUCTION

Power MOSFETs operate with gate loss equal to the product of the total gate charge, gate drive voltage and switching frequency as given by (1).

\[ P_{\text{gate}} = Q_g V_{GS} f_s \]  

(1)

Traditionally, in low power converters operating at switching frequencies below 500kHz, gate loss was considered to be small in comparison to other losses. However, in recent years as switching frequencies have increased above 500kHz and MOSFETs with lower \( R_{DS} \) ratings have been used, gate losses have increased enough that there has been a push to develop techniques to recover some, or all of the gate energy.

In the early 1990s, there was a significant amount of work published for resonant converters operating above 1MHz, and at this time several papers and patents were published proposing techniques to recover gate energy [1]-[9]. After reviewing these ideas, it can be concluded that it is desirable to design a resonant gate driver with three characteristics:

1) Zero circulating current in order to minimize conduction loss in the driver circuit during the power MOSFET on and off states
2) Quick turn-on and turn-off transition times to minimize both conduction and switching losses in the power MOSFET
3) The ability to actively clamp the power MOSFET gate to the line during the on time and to ground during the off time in order to avoid undesired false triggering of the power MOSFET gate, i.e., \( C_dv/dt \) immunity

Conventional lossy gate drive methods use a voltage source to charge and discharge the power MOSFET gate through a resistive control switch and external resistor. Energy is taken from the line to charge the gate and then sent to ground when discharging the gate. A bi-directional current pulse wave can also be used to drive the gate. This is illustrated in Fig. 1 by the second curve, \( I_{GS \text{ Desired}} \). To achieve lossless gate drive, the gate energy must be returned to the line, which can be accomplished using an inductor as temporary storage. Conveniently, an inductor can also be used as a current source to drive the gate. However, the inductor current cannot step to achieve the desired gate current source, so in the method proposed in [1], the inductor current is a continuous triangular in shape as shown by the \( I_{GS \text{ Achieved}} \) curve in Fig. 1.

![Fig. 1 Evolution of the proposed resonant gate drive circuit](image)

Other previously proposed resonant gate drive methods allow the inductor current to go discontinuous. However, they suffer from slow transition times since the power MOSFET gate capacitance begins to charge when the inductor current starts at zero. Therefore, if it is possible to combine the benefits of the two methods, namely discontinuous inductor current and relatively constant drive current in [1], then an optimal resonant gate driver can be achieved. This idea is presented in the curve labeled \( I_{LR \text{ Proposed}} \) in Fig. 1. Since the inductor current cannot step, a charging interval is used so that the current reaches a pre-charge turn-on level before directing the current to the gate. After charging the power MOSFET gate, this current can then be allowed to decrease while at the same time clamping the gate high. This idea can be implemented as shown in the following section.

II. PROPOSED CIRCUIT AND WAVEFORMS

A circuit is presented in Fig. 2 that can achieve the desired inductor current wave shape, \( I_{LR \text{ Proposed}} \) in Fig. 1. The circuit consists of four control switches and one small inductor. Switch \( Q \) represents the power MOSFET to be driven.
Fig. 2 Proposed resonant gate drive circuit

Fig. 3 can be used to explain the operation of the circuit in order to understand how the gate energy can be saved. The current paths during the four intervals of the turn-on stage are illustrated in Fig. 3 (a). The current paths during the four intervals of the turn-off stage are illustrated in Fig. 3 (b). The gating waveforms of the four control switches, \( Q_1 \)–\( Q_4 \), along with the inductor current, gate current, power MOSFET gate-to-source voltage and the line current are illustrated in Fig. 3 (c).

The operation of the circuit is explained as follows. Initially it is assumed that the power MOSFET is in the off state before time \( t_0 \). For the control switches, the shaded regions indicate the on-state, so initially only switches \( Q_3 \) and \( Q_4 \) are on and the gate of \( Q \) is clamped to zero volts. In all cases, a small deadtime (not shown) is added between the complementary transitions of \( Q_2 \) and \( Q_1 \) to eliminate shoot-through and allow ZVS, or ZCS.

**t0-t1:**
At time \( t_0 \), \( Q_4 \) turns off (with ZCS) and then \( Q_2 \) turns on (with ZCS) allowing the inductor current to ramp up. The current path during this interval is \( Q_2 - L_R - Q_3 \). Since \( Q \) is in the on state, the gate of \( Q \) is clamped low. The interval ends at time \( t_1 \).

**t1-t2:**
At time \( t_1 \), \( Q_3 \) turns off (with approximate ZVS due to large shunt power MOSFET gate capacitance), which allows the inductor current to begin to charge the power MOSFET gate. Since the dotted side of the inductor is clamped to the line and the other side is connected to the gate capacitance of \( Q \), the inductor current will continue to ramp up, but with a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is \( Q_2 - L_R - C_g \), where \( C_g \) represents the equivalent gate capacitance of \( Q \). This interval ends at time \( t_2 \), when \( v_{gs} \) reaches \( V_{CC} \). If this interval is allowed to continue, the body diode of switch \( Q_1 \) will allow the current to freewheel through \( Q_2 - L_R - BDQ_1 \).

**t2-t3:**
At time \( t_2 \), \( Q_2 \) turns off and \( Q_1 \) and then \( Q_4 \) turn-on (both with ZVS) allowing the inductor current to conduct into the dot through the path \( Q_4 - L_R - Q_4 \). Most importantly, it is during this interval when the gate charging energy is returned to the line. This can be observed from the negative portion of the \( I_{VCC} \) curve in Fig. 3. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate voltage of \( Q \) remains clamped to the line voltage, \( V_{CC} \). The interval ends when the inductor current reaches zero at time \( t_3 \).
t3-t4:
At time $t_3$, $Q_4$ turns off (with ZCS) and then $Q_2$ turns on (with ZCS), which allows any residual inductor current to freewheel through $Q_2\cdot L_R\cdot Q_4$. During this interval, the gate voltage of $Q$ remains clamped to $V_{CC}$. The interval ends at time $t_4$ when the pre-charging interval for the turn-off cycle begins as dictated by the PWM signal.

t4-t5:
At time $t_4$, the turn-off pre-charging interval begins. $Q_2$ turns off (with ZCS) and $Q_3$ turns on (with ZCS). Since $Q_f$ was previously on, the inductor current begins to ramp negative out of the dot through the path $Q_f\cdot L_R\cdot Q_4$. During this interval, the gate voltage of $Q$ remains clamped to $V_{CC}$. The interval ends at time $t_5$.

t5-t6:
At time $t_5$, $Q_1$ turns off (with shunted ZVS from $Q$), which allows the inductor current to begin to discharge the power MOSFET gate. Since the dotted side of the inductor is clamped to ground and the other side is connected to the gate capacitance of $Q$, the inductor current will continue to ramp negative with a reduced slope as the voltage across the gate capacitance decreases. The current path through this interval is $C_G\cdot L_R\cdot Q_4$, where $C_G$ represents the equivalent gate capacitance of $Q$. This interval ends at time $t_6$, when $V_{GS}$ reaches zero. If this interval is allowed to continue, the body diode of switch $Q_3$ will allow the current to freewheel through $BDQ_3\cdot L_R\cdot Q_4$.

t6-t7:
At time $t_6$, $Q_2$ turns off and $Q_1$ and $Q_2$ turn-on (both with ZVS) allowing the inductor current to conduct out of the dot through the path $Q_2\cdot L_R\cdot Q_2$. Most importantly, it is during this interval when the gate discharging energy is returned to the line. This can be observed from the negative portion of the $I_{VCC}$ curve in Fig. 3. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate voltage of $Q$ remains clamped to ground. The interval ends when the inductor current reaches zero at time $t_7$.

t7-t0:
At time $t_7$, $Q_2$ turns off (with ZCS) and $Q_4$ turns on (with ZCS), which allows any residual inductor current to freewheel through $Q_2\cdot L_R\cdot Q_4$. During this interval, the gate voltage of $Q$ remains clamped to ground. The interval ends at time $t_0$ when the pre-charging interval for the turn-on cycle begins and the entire process repeats as dictated by the PWM signal.

It can be observed from the operating intervals that energy is taken from the line during three intervals, $t_3-t_1$, $t_1-t_2$ and $t_5-t_0$, and energy is returned to the line during two intervals, $t_2-t_3$ and $t_7-t_5$. Qualitatively, if the positive and negative amp-second area products are equal, then all of the gate energy can be recovered. However, since the real circuit will have losses in the control switches, control switch pre-drivers, inductor and power MOSFET gate resistance, all of the gate energy cannot be recovered, so the positive amp-second area will be greater than the negative amp-second area.

### III. Logic Implementation

The logic required to produce the gating signals for the four control switches, $Q_1$-$Q_4$, is very simple. The logic waveforms used to create the three control signals for $Q_1$-$Q_4$ are illustrated in Fig. 4. The only logic input to the gate drive circuit is a PWM signal generated by the converter controller. In order to implement the appropriate pre-charging intervals, gate charging intervals and energy return intervals, delay circuitry is required to delay the PWM signal for the appropriate times. The delayed signals are labeled $D_1$-$D_5$. The required gating signals for $Q_1$-$Q_4$ are given after the PWM signal using the logic functions labeled $A$-$C$.

![Fig. 4 Logic waveforms used to create the control switch gating signals for $Q_1$-$Q_4$.](image)

The logic circuit used to create the three control signals for $Q_1$-$Q_4$ are illustrated in Fig. 5. Tapped delay lines can be used for the delay elements. High speed gates should be used for the logic elements. The pre-drivers consist of BJT totem-pole pairs.

![Fig. 5 Logic circuit used to create the control switch gating signals for $Q_1$-$Q_4$.](image)

### IV. Loss Analysis

The sources of loss in the proposed driver include conduction loss in the control switches, inductor and MOSFET gate resistance. In comparison to a conventional gate driver with two control switches, the proposed resonant
gate driver exhibits inductor core loss and additional gate loss in the extra two switches in the left leg, Q3 and Q4, which switch at three times the switching frequency. There is no additional switching loss in the proposed driver. In fact, since the right leg switches turn-on with ZVS, some additional energy is saved in comparison to a conventional driver.

This sub-section will focus on the conduction loss in the control switches. The additional gate loss in Q3 and Q4 can be easily calculated using (2), where \( Q_{G3} \) and \( Q_{G4} \) represent the total gate charge in switches \( Q_2 \) and \( Q_4 \). Given this additional gate loss at three times the switching frequency, it is noted that switches \( Q_2 \) and \( Q_4 \) should be chosen to minimize both their conduction loss and additional gate loss, so it is reasonable to assume that they can be selected with lower gate charge and higher on resistances than \( Q_1 \) and \( Q_3 \).

\[
P_{G3G4} = 3 f_s (Q_{G3} + Q_{G4}) V_{CC}
\]  

(2)

The equivalent circuit for loss analysis of the proposed driver is given in Fig. 6. The power MOSFET being driven is represented by an RC network consisting of its parasitic series gate resistance, \( R_G \), and an equivalent gate capacitance, \( C_G \), which is easy calculated using (3) and total gate charge data from the device datasheet. During the on state, the control switches can be represented by series resistances \( R_{3} \) and \( R_{4} \). The inductor copper loss can be represented by an equivalent series resistance, \( R_L \), which can be estimated, or obtained from the inductor datasheet.

\[
C_G = \frac{Q_G}{V_{CC}}
\]  

(3)

The conduction loss in the proposed resonant gate driver can be determined by analyzing the losses during the three main states of the turn-on interval. This is clear since the turn-off interval is symmetrical with respect to the turn-on interval, so the turn-on losses can be doubled.

The detailed inductor current waveform and power MOSFET gate voltage waveform are shown for the turn-on interval in Fig. 7. The actual inductor current waveform will follow the shape given by the solid line with a non-linear transition during the turn-on of the gate voltage. Using a piecewise linear approximation to simplify the analysis, the inductor current waveform can be approximated using the dotted portion during \( t_{on} \), so that the entire interval is given by the shaded region. The power MOSFET gate voltage will follow the solid line during turn-on, but can be approximated by the dotted line if it is assumed that the gate is driven by a constant current source of value \( I_{avg} \) during \( t_{on} \).

In Fig. 7, the inductor current pre-charge interval is labeled \( t_a \) and it occurs from time \( t_0 \) to \( t_1 \). The actual turn-on interval is labeled \( t_b \), which is also \( t_{on} \), and it occurs from time \( t_1 \) to \( t_2 \). The ramp down interval is labeled \( t_c \) and it occurs from \( t_2 \) to \( t_3 \).

It is useful to derive a few relationships before explaining the three intervals in greater detail. The first requirement is to determine, or set the turn-on time, \( t_{on} \), of the power MOSFET. This is usually dictated by the application. Once \( t_{on} \) is set, using the piecewise linear approximation during the \( t_b \) interval, the average inductor current is derived using (4), which is simplified to (5) in order to determine \( I_{avg} \).

\[
Q_G = I_{avg} t_{on} = C_G V_{CC}
\]  

(4)

\[
I_{avg} = \frac{C_G V_{CC}}{t_{on}}
\]  

(5)

In order to simplify the analysis, it is useful to define the transition time \( t_{on} \) as a fraction of the switching period, or equivalently as a multiple of the switching frequency. Using \( F \) to denote the selected fraction of the switching period, \( t_{on} \) can be expressed using (6).

\[
t_{on} = \frac{F}{f_s}
\]  

(6)

The final useful relationship is to express the ripple portion of the inductor current during \( t_{on} \). The actual equivalent circuit is complex, but since the power MOSFET gate capacitor voltage increases from zero to \( V_{CC} \) during \( t_{on} \), then the average capacitor voltage during the interval is \( V_{CC}/2 \). Using this approximation along with (6), the ripple current component, \( \Delta I_{LR} \), can be approximated using (7).

\[
\Delta I_{LR} = \frac{V_{CC} F}{2 f_s L_R}
\]  

(7)

The analysis of the three intervals is explained as follows.

The equivalent circuit during \( t_b \) is given in Fig. 8. During this interval switches \( Q_2 \) and \( Q_4 \) are on, so the circuit is a series \( RL \) circuit consisting of \( R_2, R_4, R_3 \) and \( L_R \), where the resistances \( R_2, R_3 \) and \( R_4 \) have been lumped together as \( R_L \). Since the inductor value ultimately determines the duration of the three turn-on transition time intervals and the ripple current, \( \Delta I_{LR} \), it is useful to express the power consumption, \( P_{on} \), as a function of the inductor value. It can be shown that \( t_a \)
can be expressed by (8) and $P_{a}$ can be expressed using (9).

$$t_a = \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} - \frac{V_{CC} F}{4 f_s L_R} \right)$$  \hspace{1cm} (8)

$$P_a = \frac{f_s R_b}{3} \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} - \frac{V_{CC} F}{4 f_s L_R} \right)^3$$  \hspace{1cm} (9)

Fig. 8  Equivalent circuit during the pre-charge interval $t_a$

$t_b$: The equivalent circuit during $t_b$ is given in Fig. 9. During this interval only switch $Q_2$ is on, so the circuit is a series $RLC$ circuit consisting of $R_2$, $R_L$, $R_G$ and $C_G$, where the resistances $R_2$, $R_L$ and $R_G$ have been lumped together as $R_L$. It can be shown that the power consumption, $P_{b}$, during the interval is given by (10).

$$P_b = FR_s \left[ \left( \frac{f_s Q_b}{F} \right)^2 + \frac{1}{12} \left( \frac{V_{CC} F}{2 f_s L_R} \right)^2 \right]$$  \hspace{1cm} (10)

Fig. 9  Equivalent circuit during the turn-on transition interval $t_b$

The total conduction loss in the proposed resonant gate drive circuit is two times (turn-on and turn-off) the sum of $P_a$ plus $P_b$, plus $P_c$ as given by (13).

$$P_{total} = \frac{2 f_s R_b L_R}{3} \frac{Q_a f_s}{V_{CC} F} + \frac{1}{12} \left( \frac{V_{CC} F}{2 f_s L_R} \right)^2$$

The time interval $t_c$ can be expressed as (12).

$$t_c = \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} - \frac{V_{CC} F}{4 f_s L_R} \right)$$  \hspace{1cm} (12)

The total conduction loss in the proposed resonant gate drive circuit is two times (turn-on and turn-off) the sum of $P_a$ plus $P_b$, plus $P_c$ as given by (13).

$$P_{total} = \frac{2 f_s R_b L_R}{3} \frac{Q_a f_s}{V_{CC} F} + \frac{1}{12} \left( \frac{V_{CC} F}{2 f_s L_R} \right)^2$$

$$V_{CC} \cdot R_L \cdot i_{a}(t) \downarrow \uparrow \downarrow \uparrow$$

Fig. 10  Equivalent circuit during the ramp down interval $t_c$

$$P_c = \frac{f_s}{3} R_L \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} + \frac{V_{CC} F}{4 f_s L_R} \right)^3$$  \hspace{1cm} (11)

$$t_c = \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} - \frac{V_{CC} F}{4 f_s L_R} \right)$$  \hspace{1cm} (12)

The time interval $t_c$ can be expressed as (12).

The time interval $t_c$ can be expressed as (12).

The total conduction loss in the proposed resonant gate drive circuit is two times (turn-on and turn-off) the sum of $P_a$ plus $P_b$, plus $P_c$ as given by (13).

$$P_{total} = \frac{2 f_s R_b L_R}{3} \frac{Q_a f_s}{V_{CC} F} + \frac{1}{12} \left( \frac{V_{CC} F}{2 f_s L_R} \right)^2$$

$$V_{CC} \cdot R_L \cdot i_{a}(t) \downarrow \uparrow \downarrow \uparrow$$

Fig. 10  Equivalent circuit during the ramp down interval $t_c$

$$P_c = \frac{f_s}{3} R_L \frac{L_R}{V_{CC}} \left( \frac{Q_a f_s}{F} + \frac{V_{CC} F}{4 f_s L_R} \right)^3$$  \hspace{1cm} (11)

$$P_{total} = \frac{2 f_s R_b L_R}{3} \frac{Q_a f_s}{V_{CC} F} + \frac{1}{12} \left( \frac{V_{CC} F}{2 f_s L_R} \right)^2$$

V. DESIGN PROCEDURE

The first step in the design procedure is control switch selection. The control switches should be selected in order to minimize conduction loss, while at the same time minimizing gate loss. The left leg switches, $Q_2$ and $Q_4$, should be selected with lower gate charge than the right leg switches, $Q_1$ and $Q_3$.

The goal of the design procedure is to minimize the conduction loss in the proposed circuit, which is accomplished through proper selection of the inductor. If the inductor is too small, the $L/R$ time constant will not be large enough and the inductor energy storage will not be sufficient. Furthermore, the peak current during $t_{on}$ will be too large. On the other hand, if the inductor is too large, there is excess conduction loss during the on and off times of the power MOSFET. Mathematically, this behaviour can be observed (13), which is a function of $(1/L_R)^2+L_R$, which as a function of $L_R$ contains a minimum value. The minimum value can be easily found by differentiating (13) with respect to $L_R$, setting the result equal to zero and then solving for the real and positive value of $L_R$. This value of inductance is given by (14), which can easily be evaluated using a mathematical software package for the given operating condition and control switches.

$$t_a = \frac{V_{CC}}{2 f_s} \left( \frac{(R_2+R_1)^2+(4R_1+R_2-R_1)^2-2(R_2^2+4R_1^2+2R_1 R_2)R_2^2}{(R_2+R_1)^2(4R_1+R_2-R_1)^2} \right)^{1/2}$$  \hspace{1cm} (14)

After calculating the optimal inductor value, the delay times $t_{on}$, $t_b$ and $t_c$ should be calculated using (8), $t_{on}$ and (12) in order to determine the required delay times for the control logic.

VI. DESIGN EXAMPLE

A switching power converter is designed to operate at 1.5MHz to deliver power to a 35A load at 1V. Two pairs of synchronous rectifier (SR) power MOSFETs are used in the rectifier stage. The peak reverse voltage on the SRs is 4V and their gates are driven by a 5V source. The power MOSFETs, $Q_1$ and $Q_2$, and control switches, $Q_3$ and $Q_4$, were selected and their relevant parameters are given in Table 1. The turn-on transition time was selected to be 10% of the switching period, corresponding to $F=0.1$.

<table>
<thead>
<tr>
<th>Switch</th>
<th># Req Per Driver</th>
<th>Part #</th>
<th>$V_{Gns}=4.5V$</th>
<th>$V_{Gns}=4V$</th>
<th>$V_{Gns}=5V$</th>
<th>$R_G$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>2</td>
<td>IRF6691</td>
<td>2(40)=80</td>
<td>NA</td>
<td>NA</td>
<td>0.62–0.3 (R_1)</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>1</td>
<td>FDN342F</td>
<td>0.062 (R_1)</td>
<td>NA</td>
<td>NA</td>
<td>3.15</td>
</tr>
<tr>
<td>$Q_3$</td>
<td>1</td>
<td>SI5855D</td>
<td>0.160 (R_2)</td>
<td>NA</td>
<td>NA</td>
<td>1.35</td>
</tr>
<tr>
<td>$Q_4$</td>
<td>1</td>
<td>FDN335N</td>
<td>0.100 (R_2)</td>
<td>NA</td>
<td>NA</td>
<td>1.05</td>
</tr>
</tbody>
</table>

Using the parameters in the tables along with (14), the optimal inductance value is $L_R=170\mu H$. The required transition times were calculated to be $t_{on}=24ns$ using (8), $t_{on}=ton=67ns$ using (6) and $t_{on}=58ns$ using (12), corresponding to required delay times of $t_{f}=24ns$ ($t_{on}$), $t_{c}=90ns$ ($t_{on}+t_{cb}$) and $t_{c}=149ns$ ($t_{on}+t_{cb}+t_{b}$) for the PWM signal. Circuit parameters used to calculate the optimal inductance value and conduction loss are summarized in Table 2.

<table>
<thead>
<tr>
<th>Table 2</th>
<th>Switch parameters for the resonant gate driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>2(40)=80</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>0.062 (R_1)</td>
</tr>
<tr>
<td>$Q_3$</td>
<td>0.160 (R_2)</td>
</tr>
<tr>
<td>$Q_4$</td>
<td>0.100 (R_2)</td>
</tr>
<tr>
<td>$Q_5$</td>
<td>0.055 (R_3)</td>
</tr>
<tr>
<td>$Q_6$</td>
<td>1.75 (R_4)</td>
</tr>
</tbody>
</table>

654
Table 2 Additional circuit parameters for the resonant gate driver

<table>
<thead>
<tr>
<th>Label</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>5V</td>
</tr>
<tr>
<td>(F)</td>
<td>0.1</td>
</tr>
<tr>
<td>(f_s)</td>
<td>1.5MHz</td>
</tr>
<tr>
<td>(R_c)</td>
<td>0.05Ω</td>
</tr>
<tr>
<td>(R_{c1})</td>
<td>(R_{c2}+R_{c3}=0.265Ω)</td>
</tr>
<tr>
<td>(R_{c2})</td>
<td>(R_{c1}+R_{c3}=0.51Ω)</td>
</tr>
<tr>
<td>(R_{c3})</td>
<td>(R_{c1}+R_{c2}=0.212Ω)</td>
</tr>
</tbody>
</table>

The total conduction loss in the driver is 194mW, calculated using (13). The additional gate loss attributed to \(Q_2\) and \(Q_4\) is 54mW, calculated using (2). Since two drive circuits are required for the converter because there are two pairs of SRs, the total conduction loss and additional gate loss quantities are be doubled and therefore become 388mW and 108mW, respectively. The total loss using the proposed method would be 496mW. The total gate loss using conventional gate drivers would be 1.2W, calculated using (1) with four IRF6691 SRs in the rectifier. Therefore, if the core loss of the inductors is neglected, the efficiency of the proposed gate drivers is 59%. The total power savings is 0.7W for the given application, which represents 2% of the total load power, which is significant given the high operating efficiencies of present day converters.

It is also noted that the results given are for a 5V gate drive voltage. Since many converters operate with 12V gate drive voltage, gate loss can be several watts. In this case, with approximately 60% energy recovery, several watts can be saved.

One final point to note is that the greatest source of loss is due to the power MOSFET internal gate resistance, \(R_{c}\). Since power MOSFETs use a poly gate material, the gate resistance is high. In the RF field, metal gate connections are often used to minimize gate loss. If this technology is adopted for power MOSFETs, the energy savings of the proposed driver will improve significantly.

VII. SIMULATION RESULTS

SIMetrix 5.0 was used to simulate the proposed resonant gate driver. The same parameters were used as given in the design example in the previous sub-section. The simulation waveforms are given in Fig. 11. The average line current was measured to be 40mA, which represents a total loss in the circuit of 200mW, which agrees with the value of 194mW calculated in the previous sub-section.

VIII. CONCLUSIONS

A new resonant gate drive circuit has been proposed that solves all three of the problems common to existing resonant gate drivers. These problems include: 1) high conduction losses during the on and off states of the switch being driven, 2) slow turn-on and turn-off transitions due to the use of an inductance in series with the charging circuit, which begins charging and discharging the gate with zero initial current, and 3) a lack of \(Cdvd\)t immunity due to a lack of active clamping at the gate of the device being driven. Furthermore, the inductor used in the proposed method is quite small and is typically about one third of the size of the inductor required in [1].

The logic circuit required to generate the control switch gating signals has also been presented. A simple design procedure has been included in this section in order to determine the optimum inductor value and delay times. A loss analysis and design example has also been presented in addition to simulation results. Good agreement was achieved between the loss analysis calculations and simulation results.

Since the inductor current is discontinuous, the proposed driver can be used for power MOSFETs operating with duty cycle control, phase shift control, asymmetrical control and variable frequency control.

REFERENCES