A New Resonant Gate Drive Circuit with Center-Tapped Transformer

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1. Introduction

2. Proposed Resonant Gate Drive Circuit

3. Analysis and Design Guidelines

4. Experimental Results

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1. Introduction

• Increased demand for higher switching frequencies:
  – Size reduction
  – Fast loop response
• BUT, Gate loss increases with frequency!
• Drawbacks of conventional gate drivers:
  – Gate charge completely lost
  – Driver overheating
  – Slow RC discharge turn-off: SWITCHING LOSS
Presentation Overview

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2. *Proposed Resonant Gate Drive Circuit*

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2. Proposed Resonant Gate Drive Circuit
Operating Principles

Before $t_1$:

1. $S_1$ and $S_3$ on
2. $M_1$ off, $M_2$ on
3. Gate voltage of $M_2$ at twice of $V_{cc}$
t1 ~ t2:
1. S3 turned off at t1
2. Magnetizing current discharges Cg of M2
3. M2 turned off
4. S2 is turned on at ZVS
t2 ~ t3:

1. At t2, S1 turned off
2. Magnetizing current charges Cg of M1
3. Vg of M1 is charged to twice of Vcc
4. Body diode of S3 conducts current
Operating Principles

After t3:

1. At t3, S3 turned on at ZVS
2. M1 on, M2 off
3. Gate voltage of M1 at twice of Vcc
Advantages

• Current source to charge and discharge the gate capacitance
  – **Switching loss can be reduced!**

• $V_{gs} = 2V_{cc}$
  – Conduction loss is reduced
  – Logic level source for $V_{cc}$

• Drives a pair of MOSFETs
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**Resonant Gate Driver Loss Components**

\[ P_{gr} = P_{rms} + P_{drive} + P_{core} \]

1. **Conduction loss – main contributor**
2. **Control switch driving loss – small share**
   - Select low gate charge control switches while conscious of \( R_{ds} \) conduction loss
   - **ZVS for control switches**
3. **Core loss – small share**
Conduction Loss Analysis

Conduction loss calculation:

\[ P_{\text{rms}} = I_{\text{ss\_rms}}^2 \cdot (2R_{\text{ds\_on}} + R_L) + 2 \cdot I_{\text{t\_rms}}^2 \cdot (R_g + 2R_L + R_{\text{ds\_on}}) \]

\[ I_{\text{ss\_rms}} = \frac{I_{pk}}{\sqrt{3}} \]

\[ I_{\text{t\_rms}} = \frac{I_{pk}}{2} \cdot \sqrt{\frac{T_t}{T_s}} \]

Relationship between driving speed and driving current:

\[ I_{pk} = \frac{4 \cdot V_{CC} \cdot C_g}{T_t} \]
• Center tapped transformer
• Bifilar wire winding construction to minimize leakage inductance impact
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Experimental Results:
$V_{cc}=5V$, $1$MHz, $L_m=900nH$, 2-FDS4410

**Recovery:**
- 48% loss saving
  - 2-FDS4410 paralleled
- 64% loss saving
  - $R_g=0.22\Omega$, $C_g=3.9nF$
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5. Conclusions

• A new resonant gate drive circuit was introduced
• Circuit drives a pair of MOSFETs
• Driving voltage is twice Vcc
• Approximately 50% gate energy recovery